

# Y12A INTEL SYSTEM DIAGRAM

<b>+3VS5/+5VS5</b>	PG.29
<b>+1.05V/+1.5V</b>	PG.30
<b>CPU Core</b>	PG.32
<b>DDR3L</b>	PG.31
<b>Charger</b>	PG.28

<b>SODIMM1</b> Max . 8GB STD PG.12	1600MT/s DDR3 L Channel A
<b>SODIMM2</b> Max . 8GB STD PG.13	1600MT/s DDR3 L Channel B

**Intel Bay Trail-M**

Power : 5 (Watt)

Package : BGA1170

Size : 25 X 27 (mm)



PG.2~11

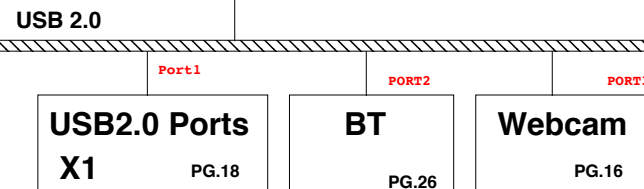
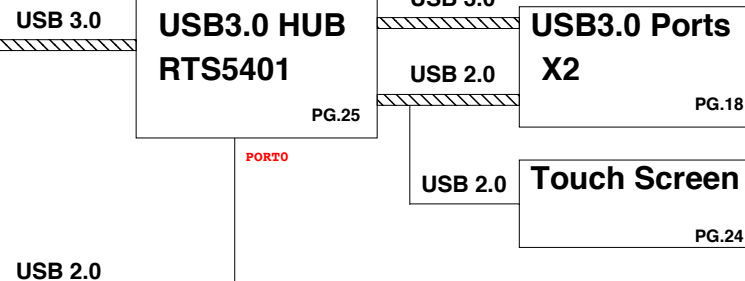
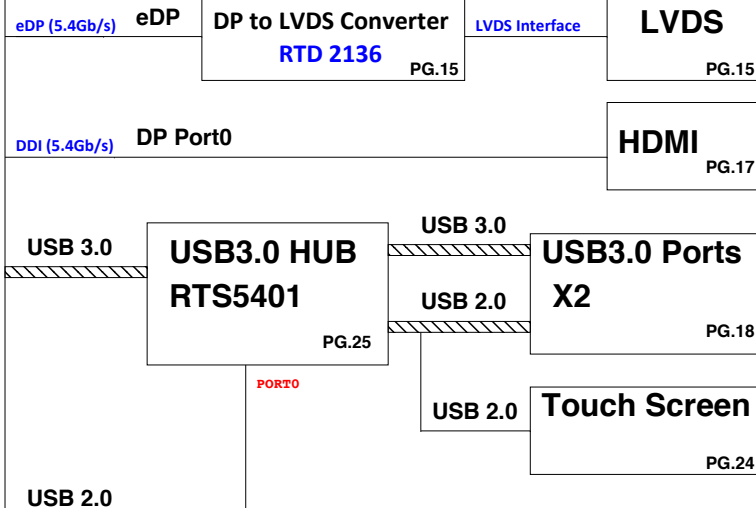
Azalia

**AUDIO CODEC**  
ALC 3227

PG.18

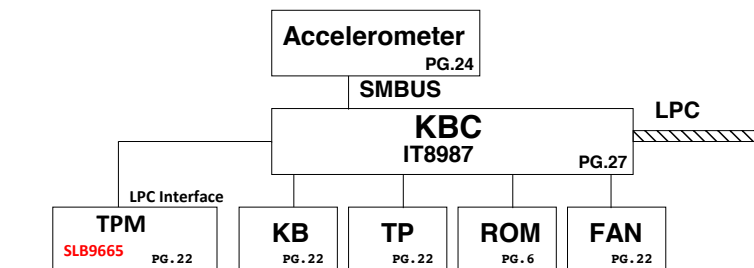
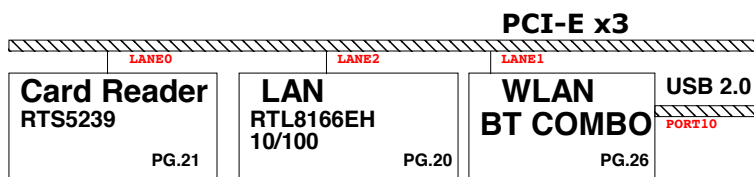
**Speaker**

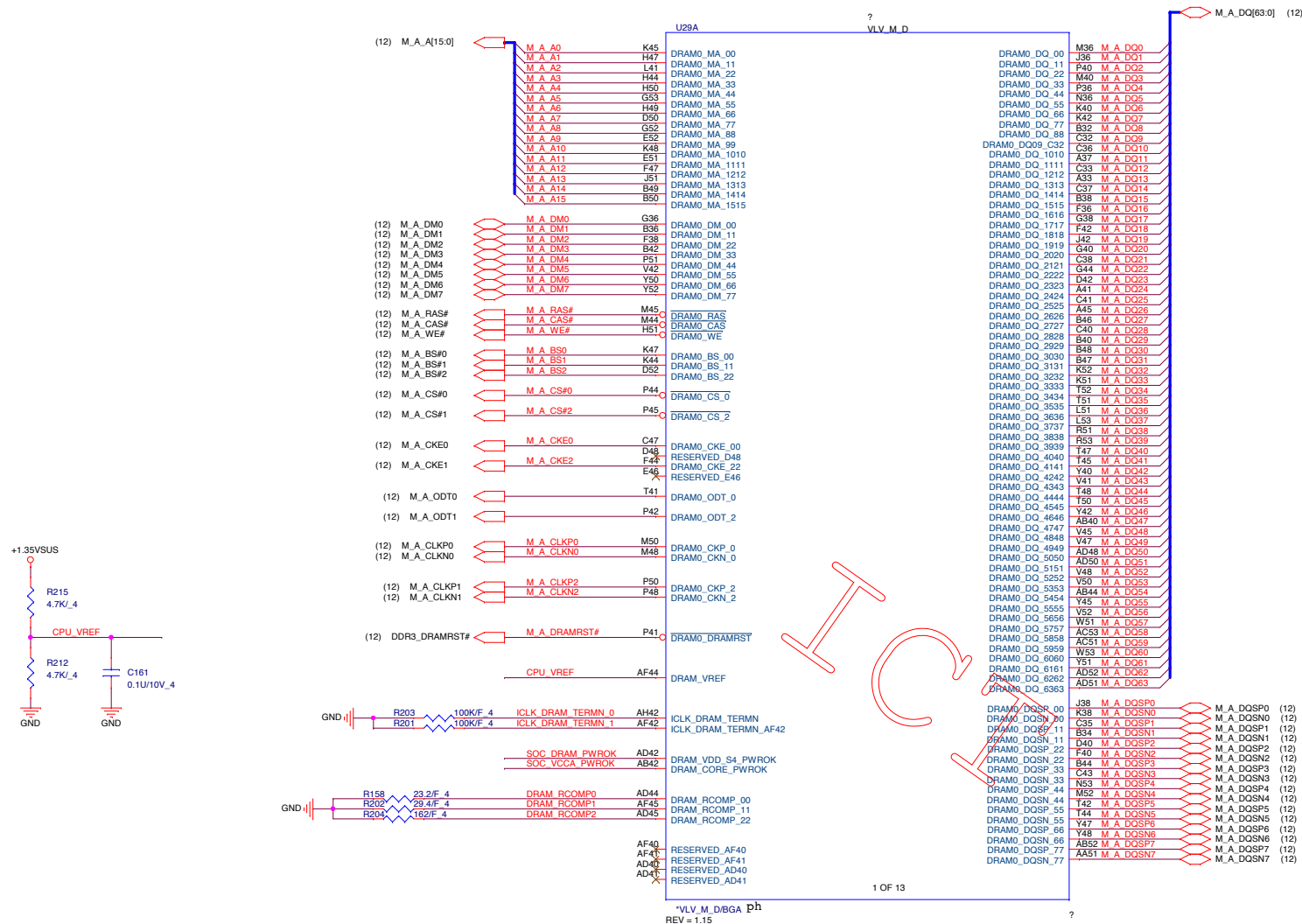
PG.18

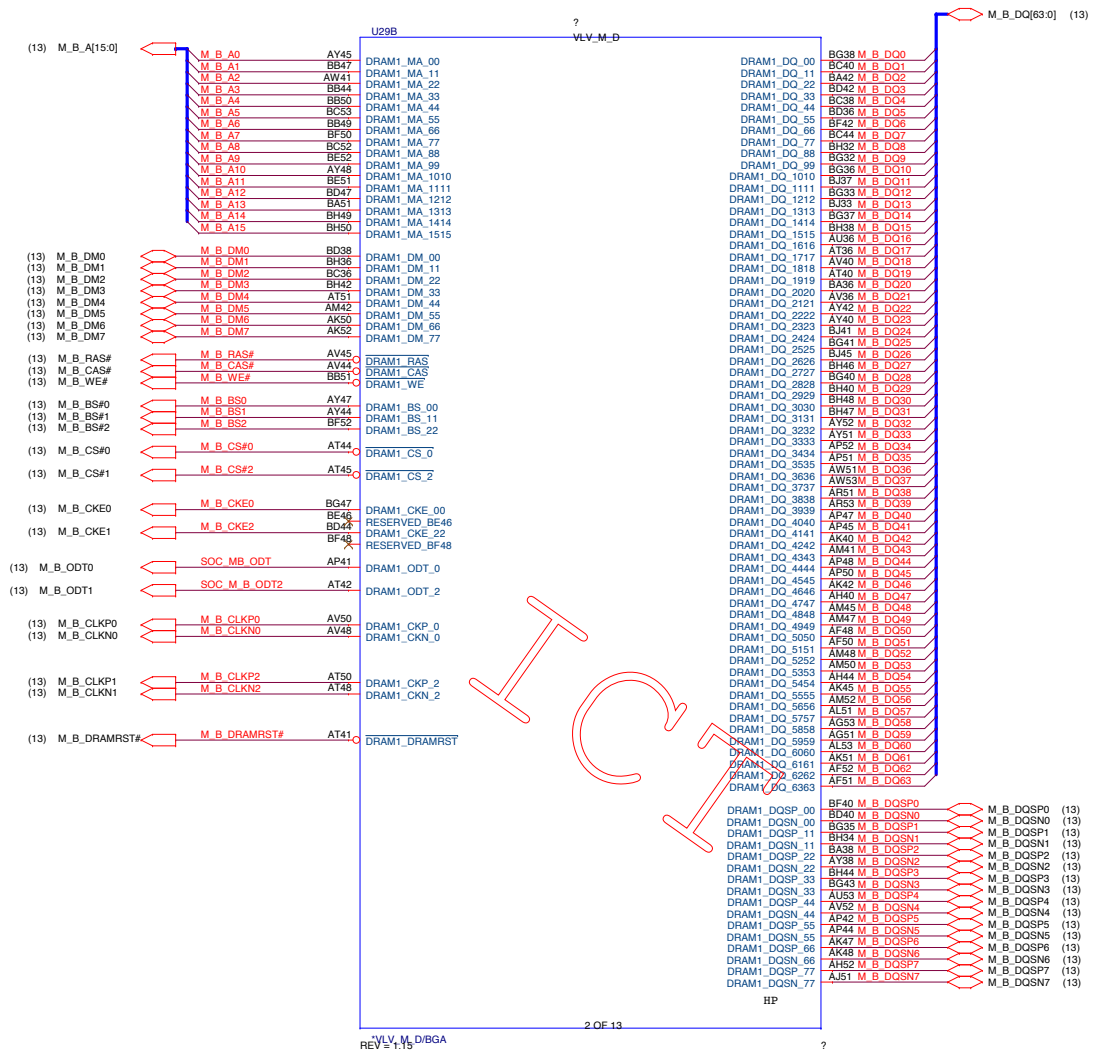


**Stackup**

TOP  
GND  
IN1  
IN2  
VCC  
BOT



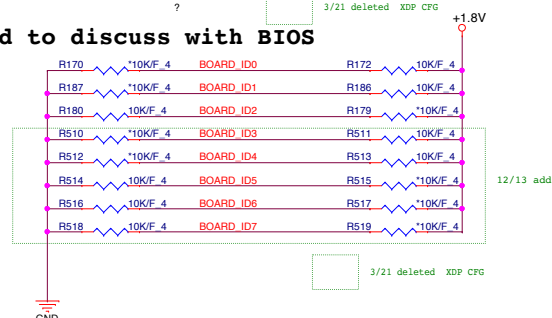


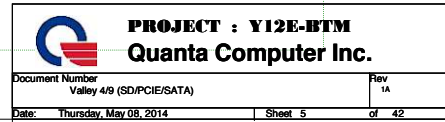


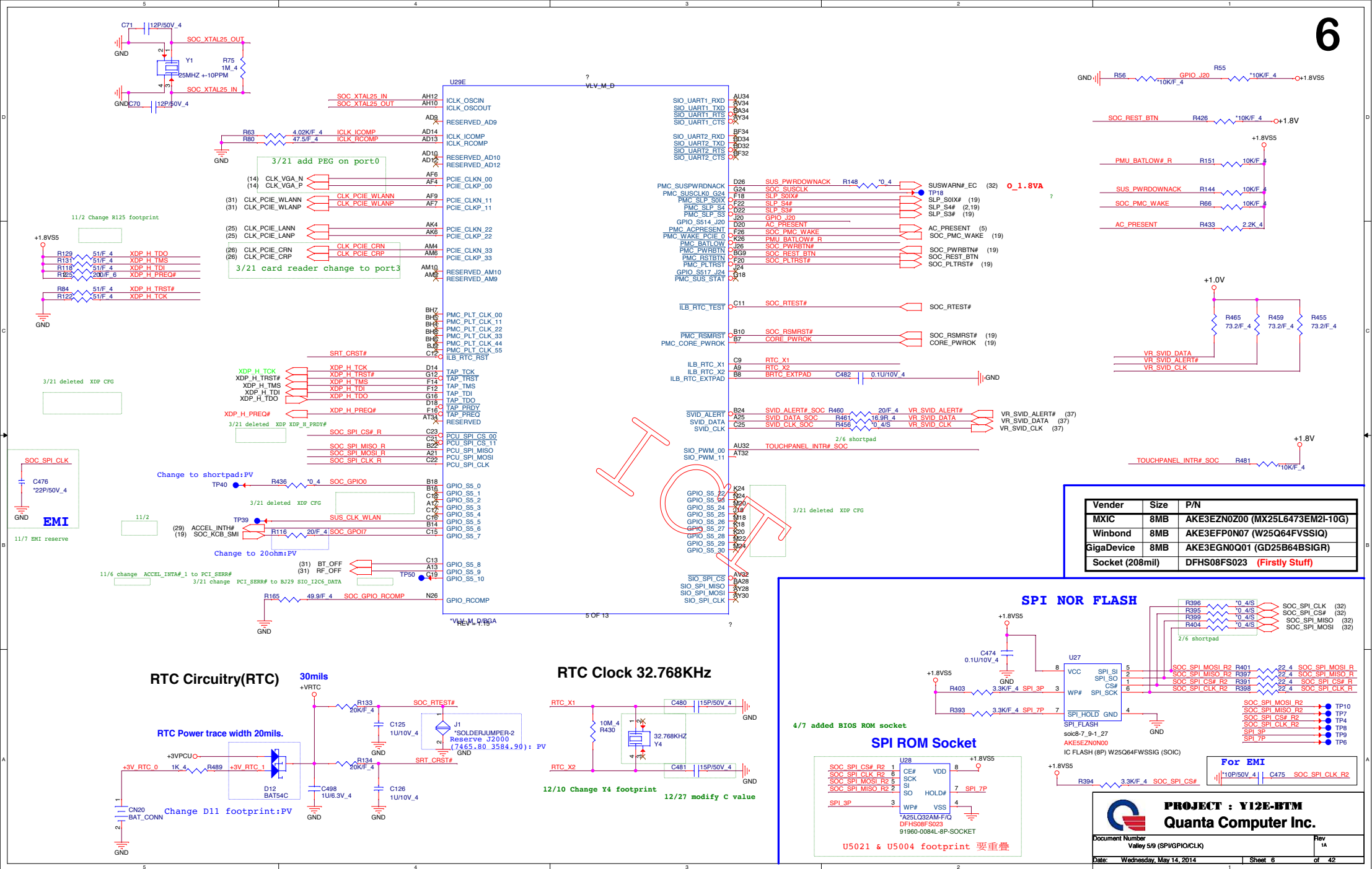


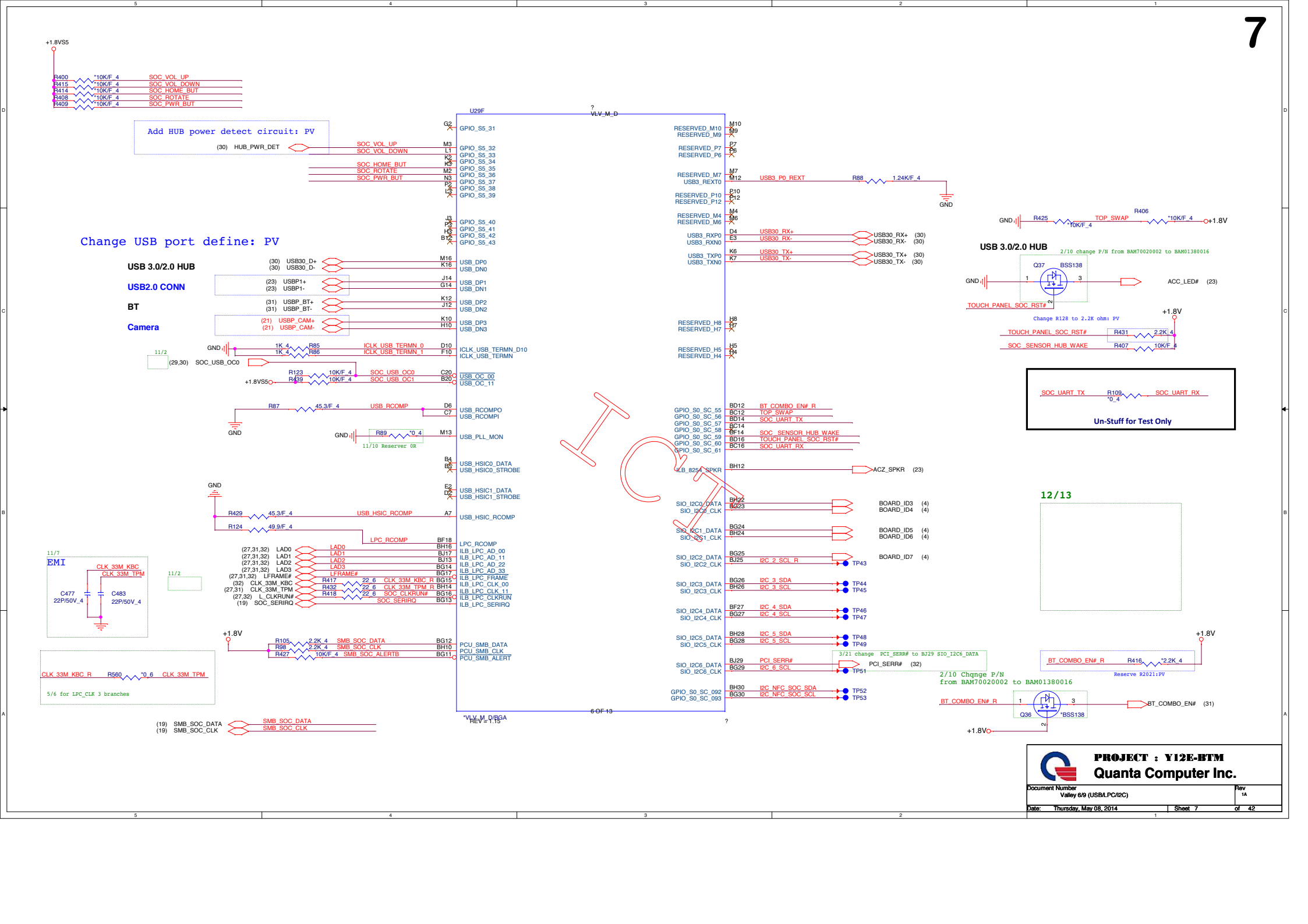
	Reserve (Default = 000)			Pavilion/Envy 00 = Pavilion 01 = Envy 10 = Pavilion Special Edition 11 = Y12E Pavilion		14" = 00 15" = 01 17" = 10		UMA=0 S.G =1
Model	BOARD_ID7	BOARD_ID6	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
Pavillion 14"	0	0	0	1	1	0	0	1
Pavillion 15.6"	0	0	0	1	1	0	1	1
Pavillion 17"	0	0	0	1	1	1	0	1

Need to discuss with BIOS





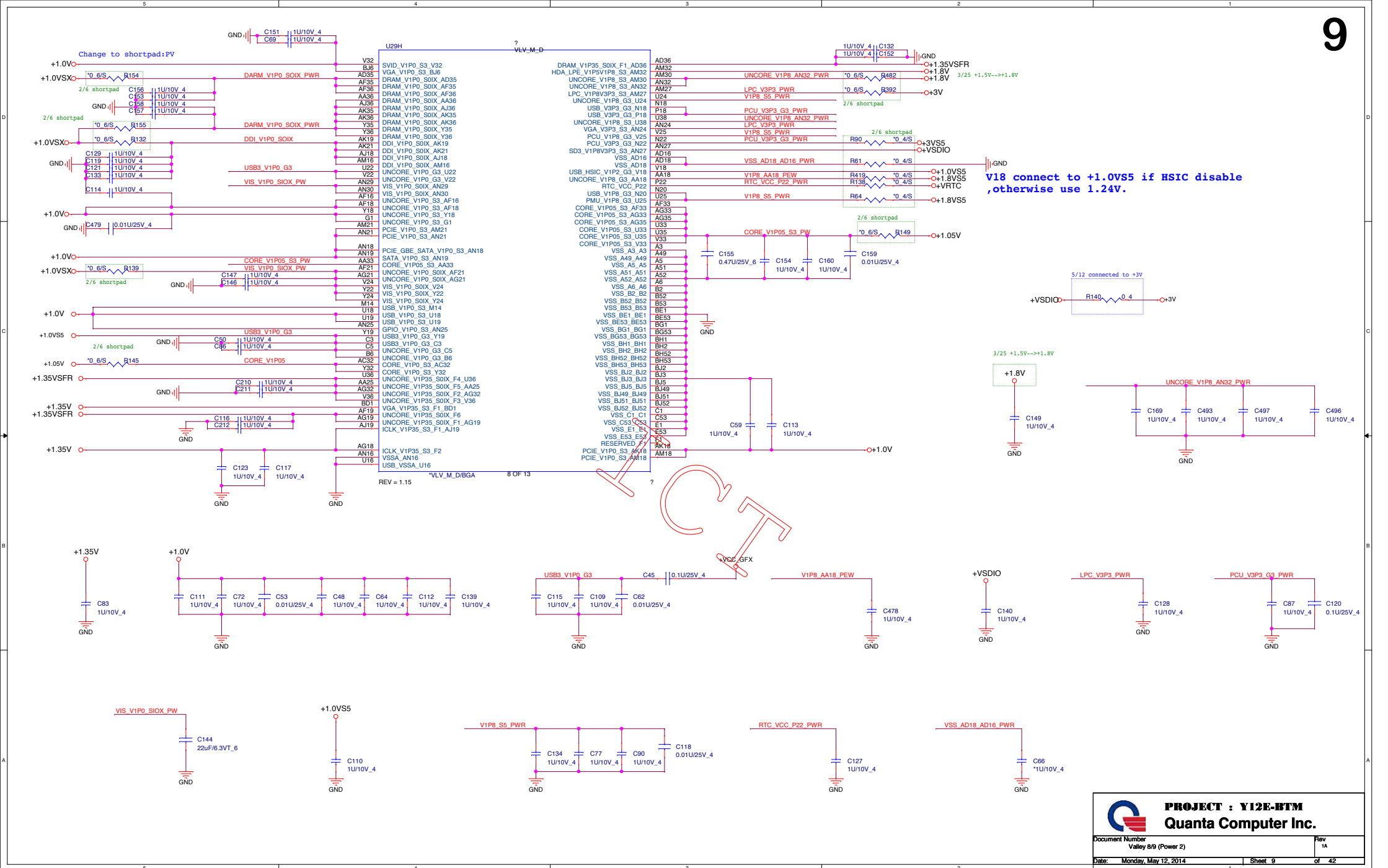


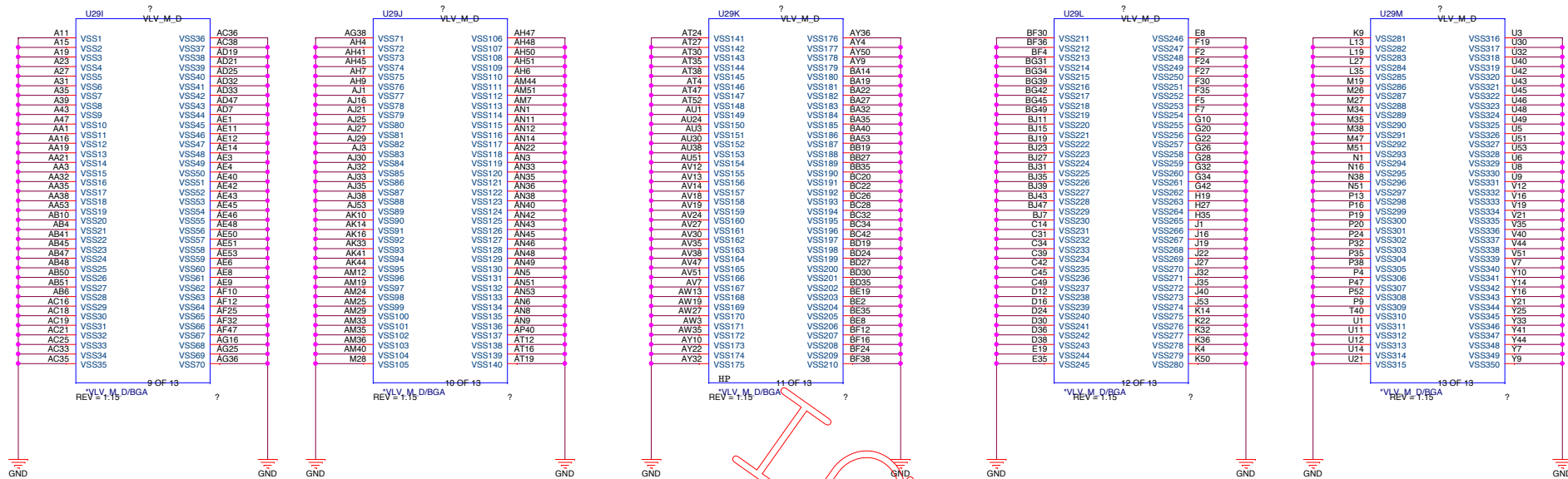






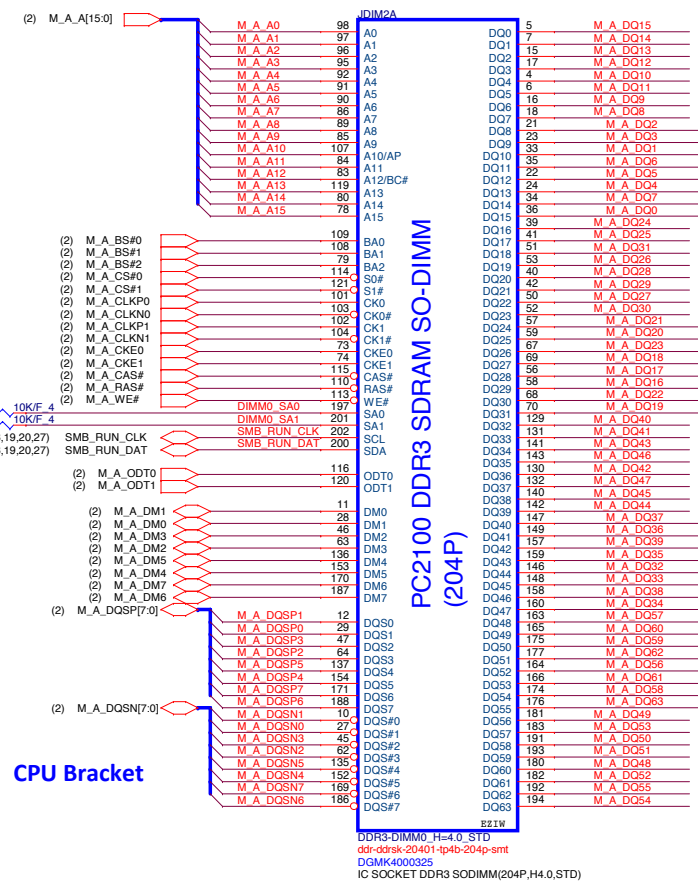




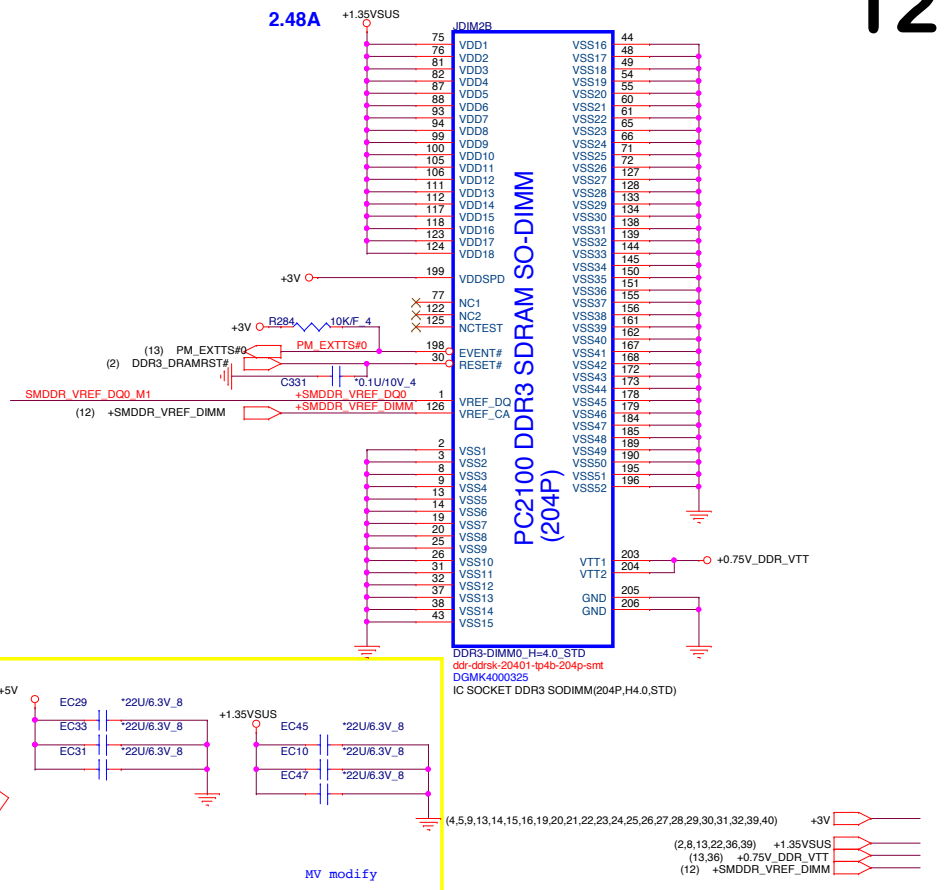


3/21 deleted XDP CH6

ICT

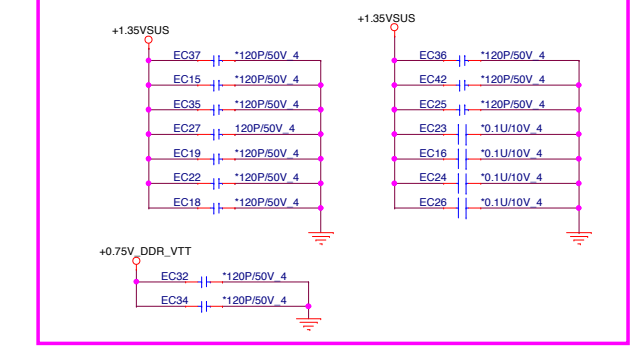


M\_A\_DQ[63:0] (2)

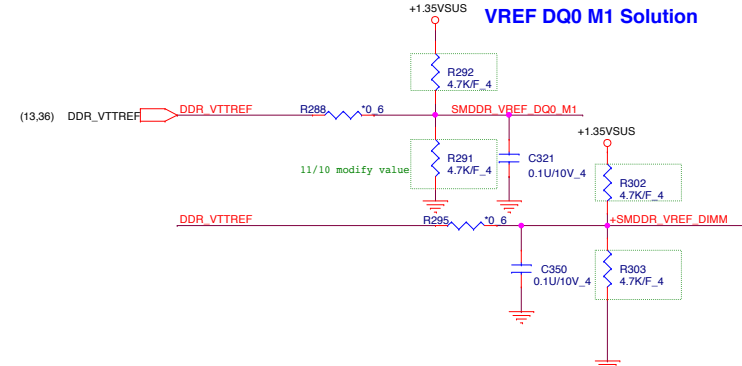
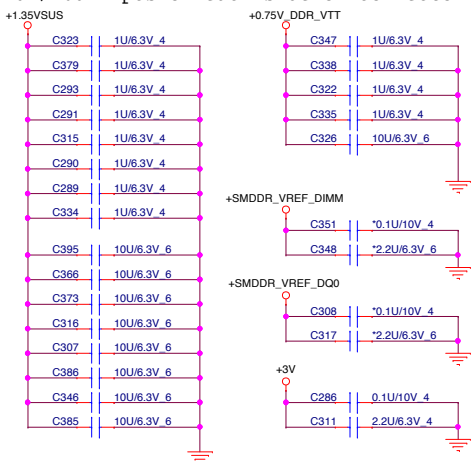


CPU Bracket

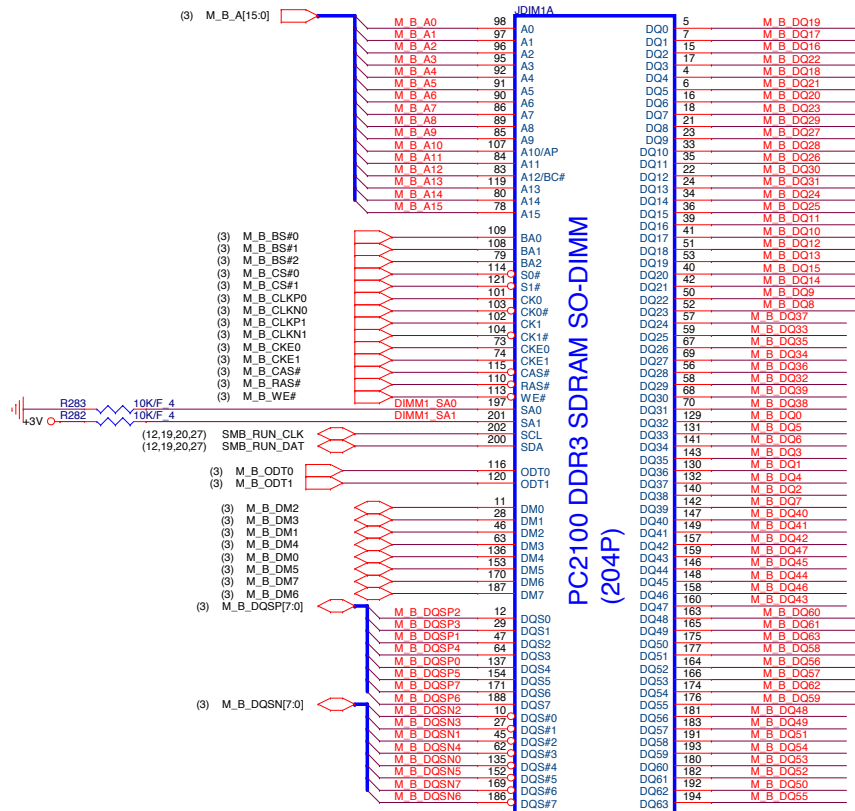
For EMI RESERVE



Place these Caps near So-Dimm0.  
1uF/10uF 4pcs on each side of connector

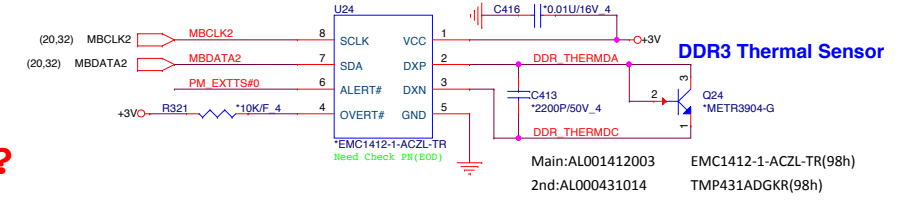


M\_B\_DQ[63:0] (3)



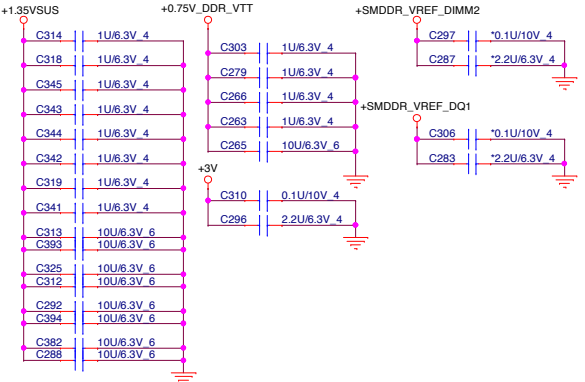
DDR3-DIMM0\_H=4.0.STD  
ddr-ddrsk-20401-tp4b-204p-smt  
DGMK4000325  
IC SOCKET DDR3 SODIMM(204P,H4.0,STD)

### Local Thermal Sensor

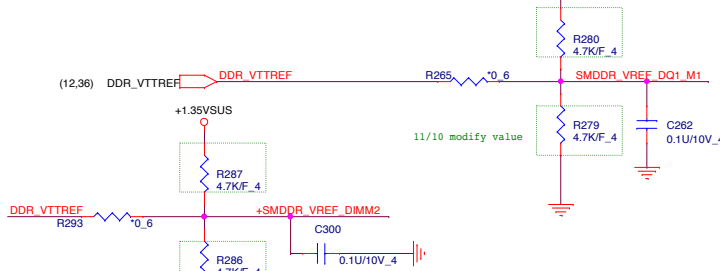



### Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



### VREF DQ1 M1 Solution



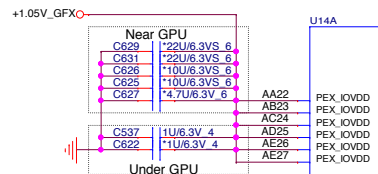
**PROJECT : Y12E-BTM**  
**Quanta Computer Inc.**

Document Number  
DDR3 DIMM1-STD(4.0H)

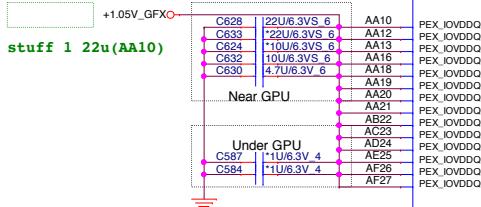
Date: Thursday, May 08, 2014

Rev 1A

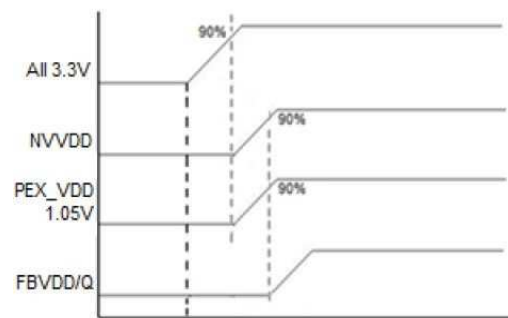
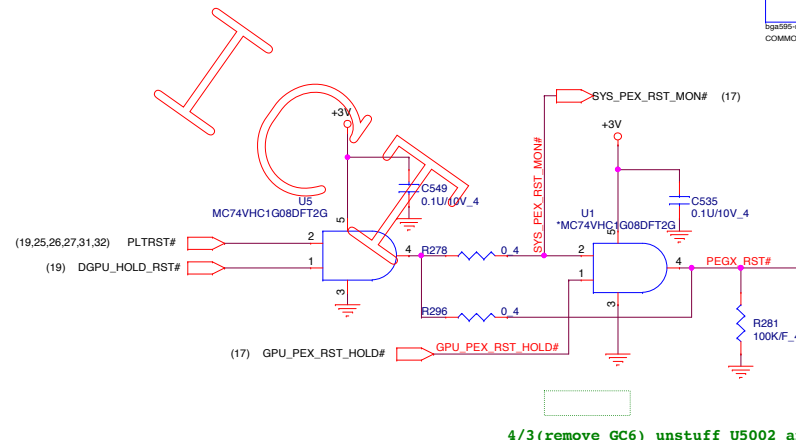
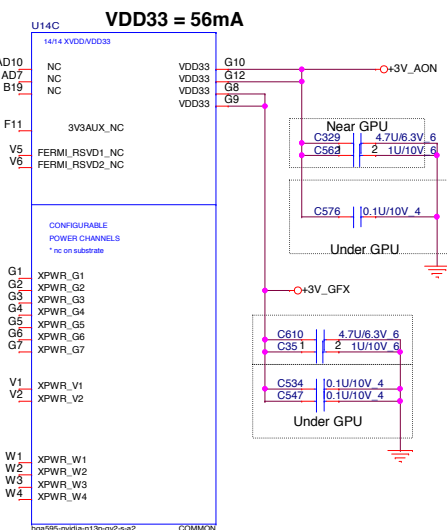
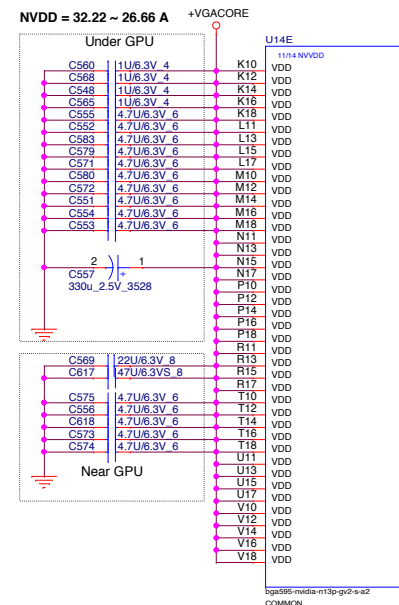
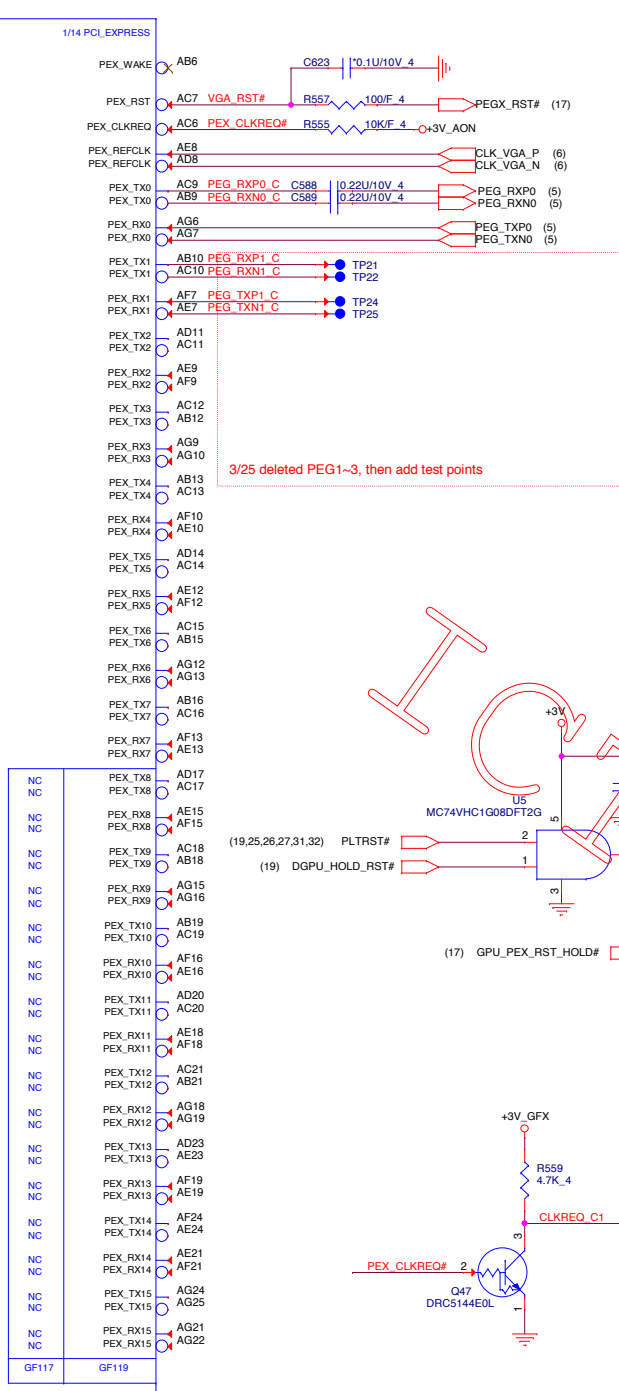
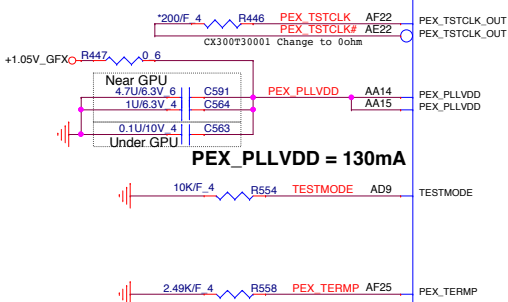
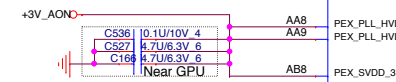
Sheet 13 of 42



**PEX\_IOVDD + PEX\_IOVDDQ = 1.042A**



**PEX\_PLL\_HVDD +  
PEX\_SVDD\_3V3 = 143mA**

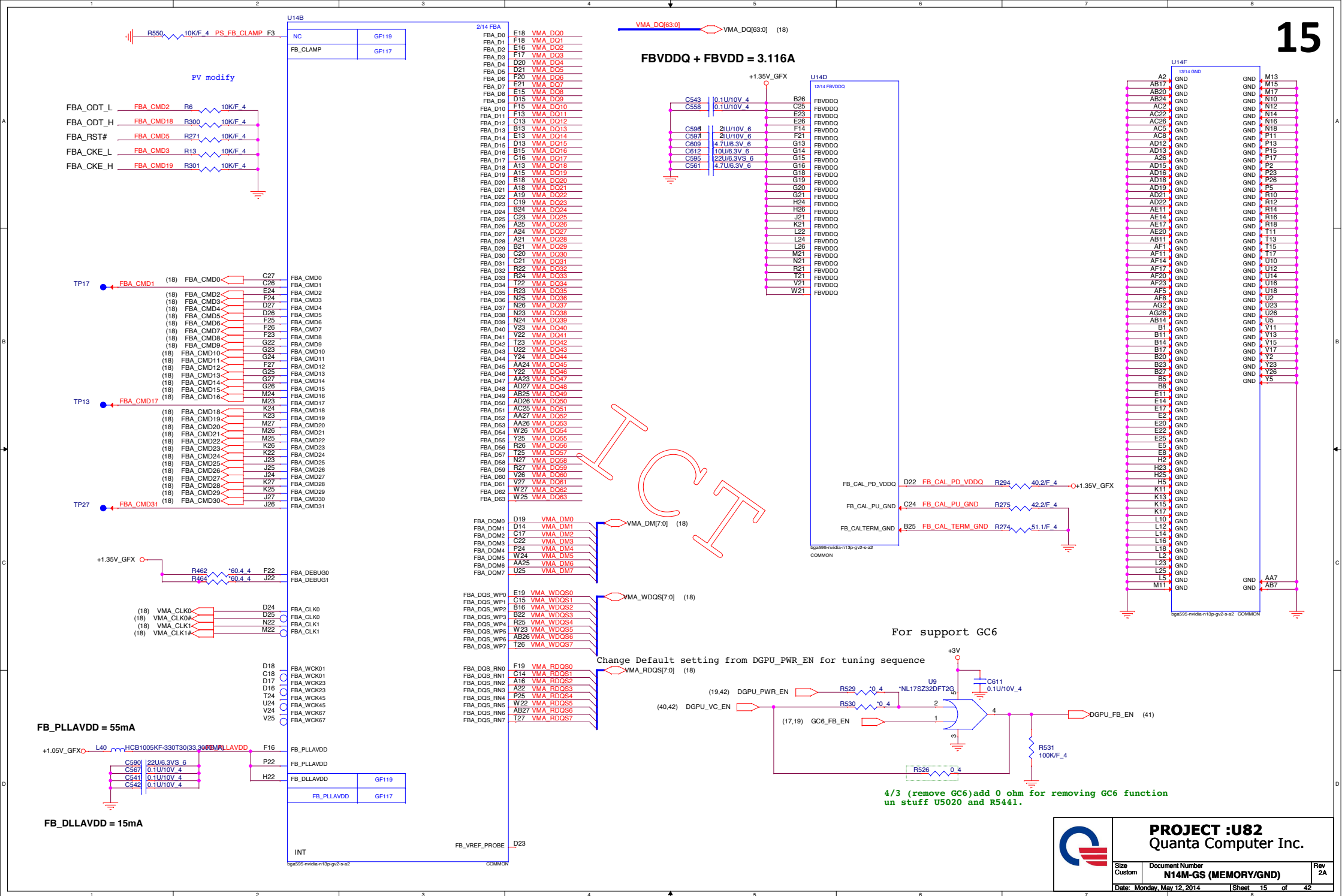


4/3(remove GC6) unstuff U5002 and stuff R5081 for PEGX\_RST#.

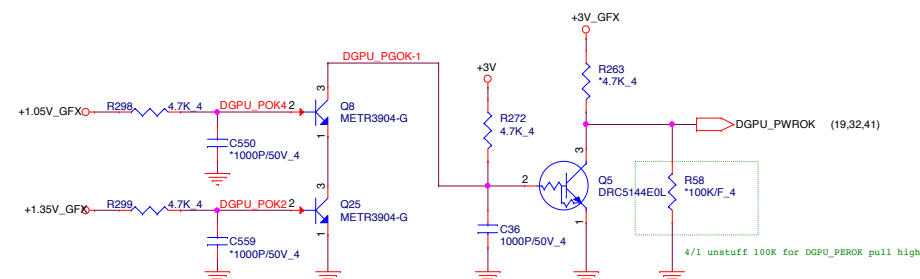
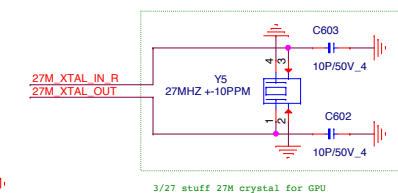
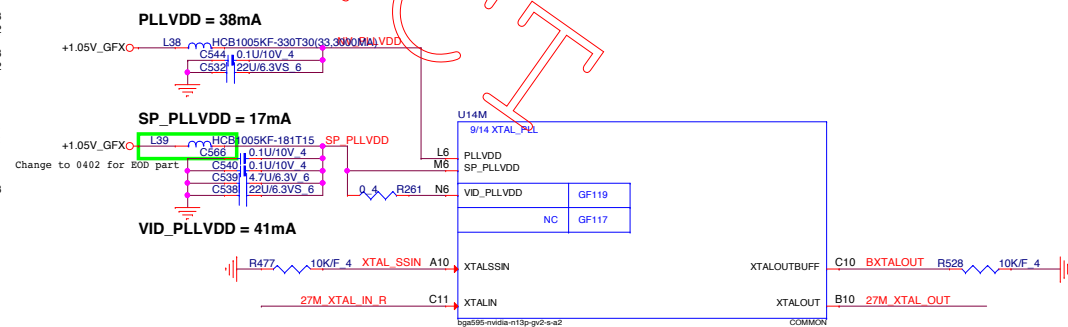
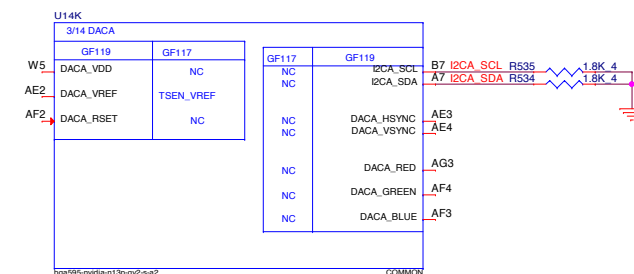
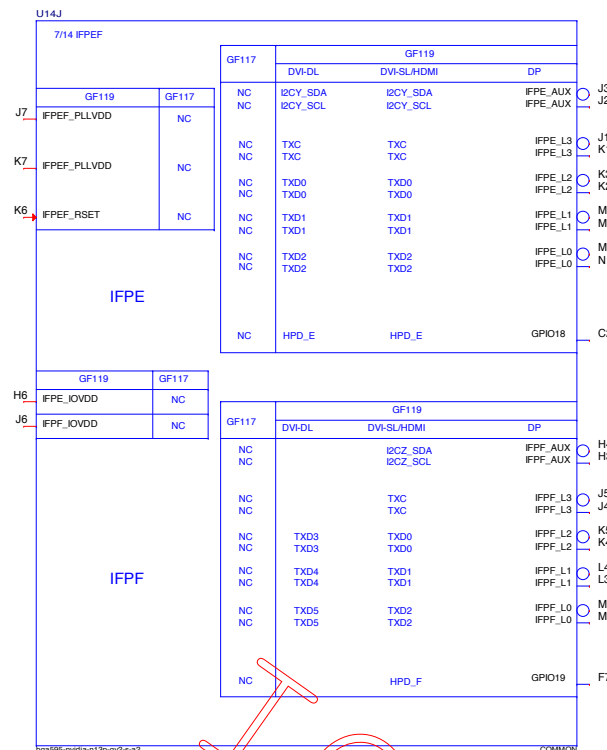
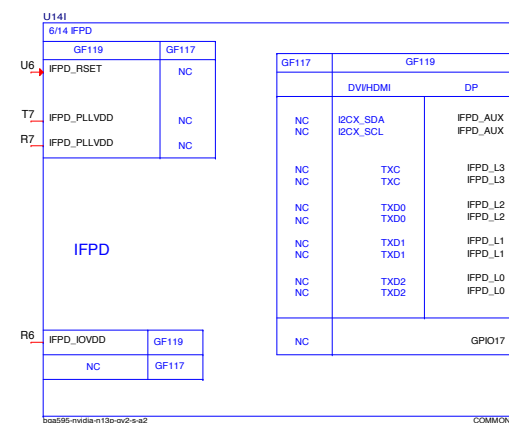
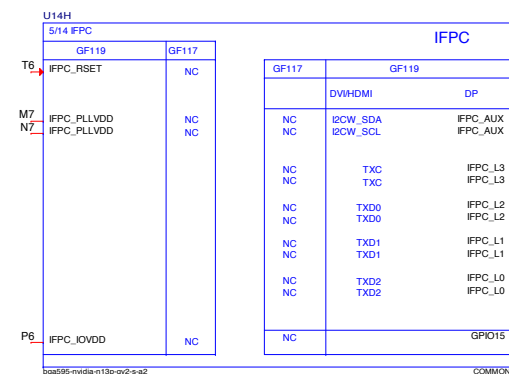
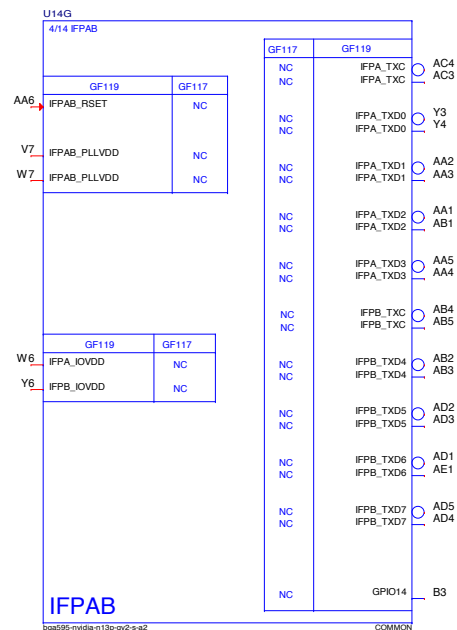


**PROJECT :U82**  
Quanta Computer Inc.

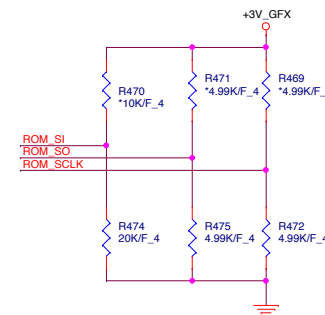
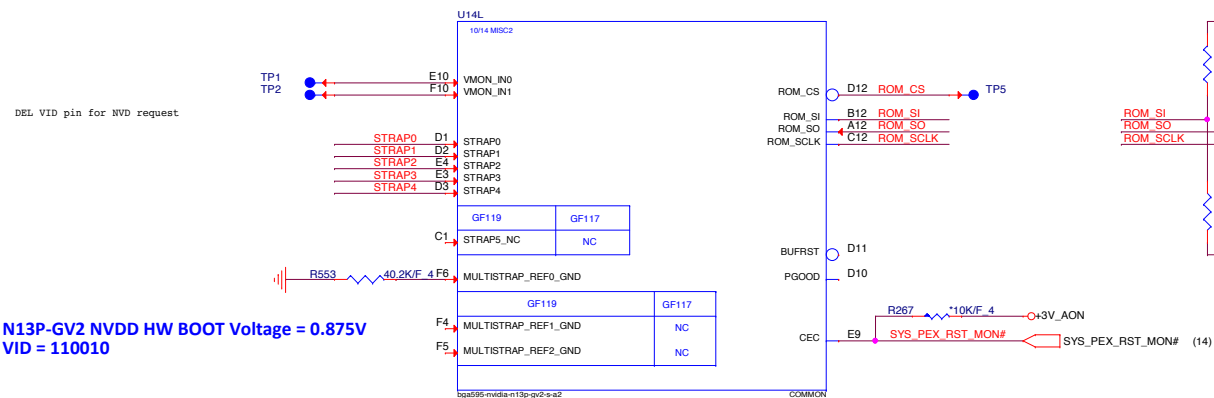
Size Custom	Document Number <b>N14M-GS (PCIE I/F) /NVDD</b>	Rev 2A
Date: Friday, May 16, 2014		Sheet 14 of 42



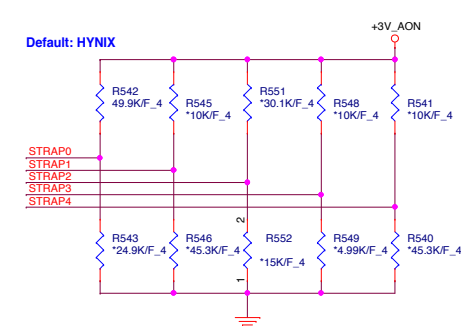




N13P-GV2 NVDD HW BOOT Voltage = 0.875V  
VID = 110010



Default: HYNIX

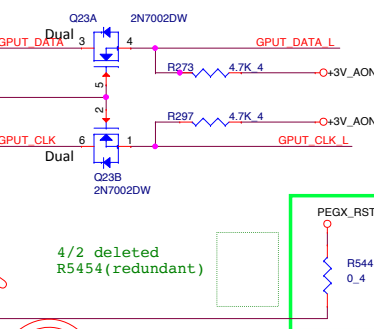
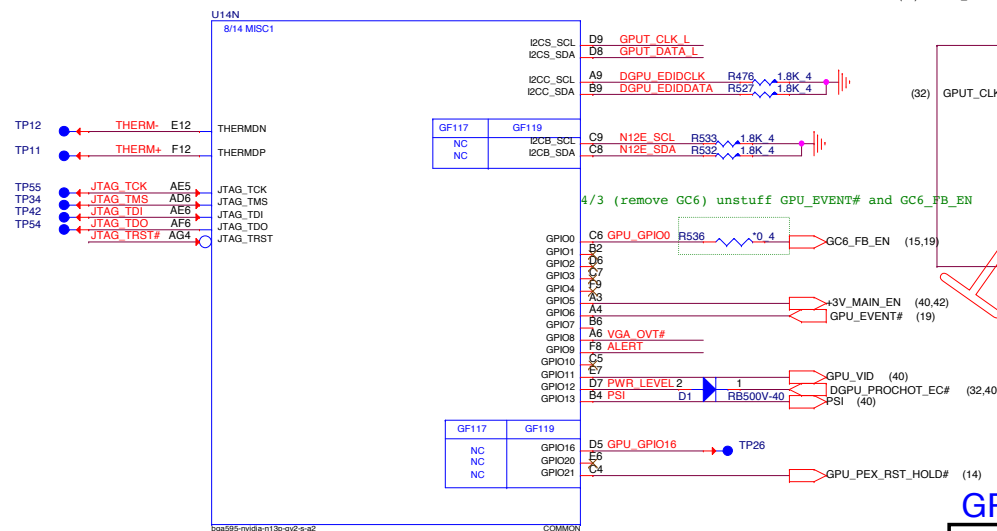


4.99k CS24992FB26  
10k CS31002FB26  
15k CS31502FB24  
20k CS32002FB29  
24.9k CS32492FB16  
30.1k CS33012FB18  
34.8k CS33482FB22  
45.3k CS34532FB18

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Hynix should be 0x3, R440 20K 1%  
Micro Should be 0x4, R440 24.9K 1%  
Samsung Should be 0x5, R440 30.1K 1%

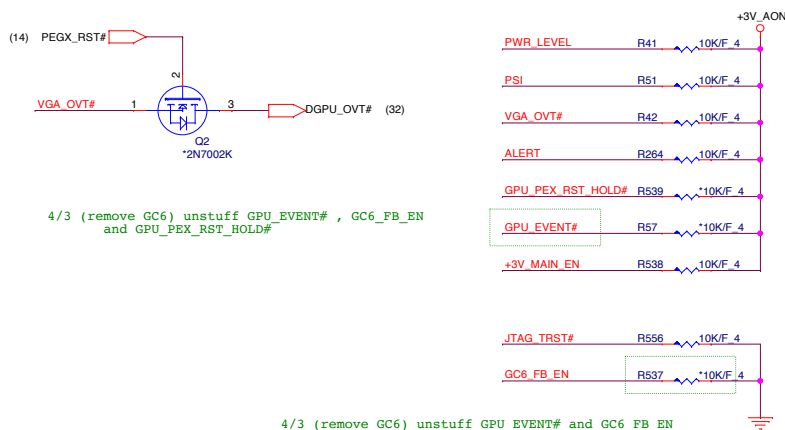


VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	QBC	TOP B/S
0000	DDR3 256Mx16, 64bit, 4Gb, 900MHz	Micron	MT41J256M16HA-093G:E	AKD5PGWT500	AKD5PZSTL01	AKD5PZSTL00
0100	DDR3 256Mx16, 64bit, 4Gb, 900MHz	HYNIX	H5TC4G63AFR-11C	AKD5PGWTW08	AKD5PGWTW07	
0011	DDR3 256Mx16, 64bit, 4Gb, 900MHz	SAMSUNG	4W4G1646D-BC1A			
0101	DDR3 256Mx16, 64bit, 4Gb, 900MHz					

## GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

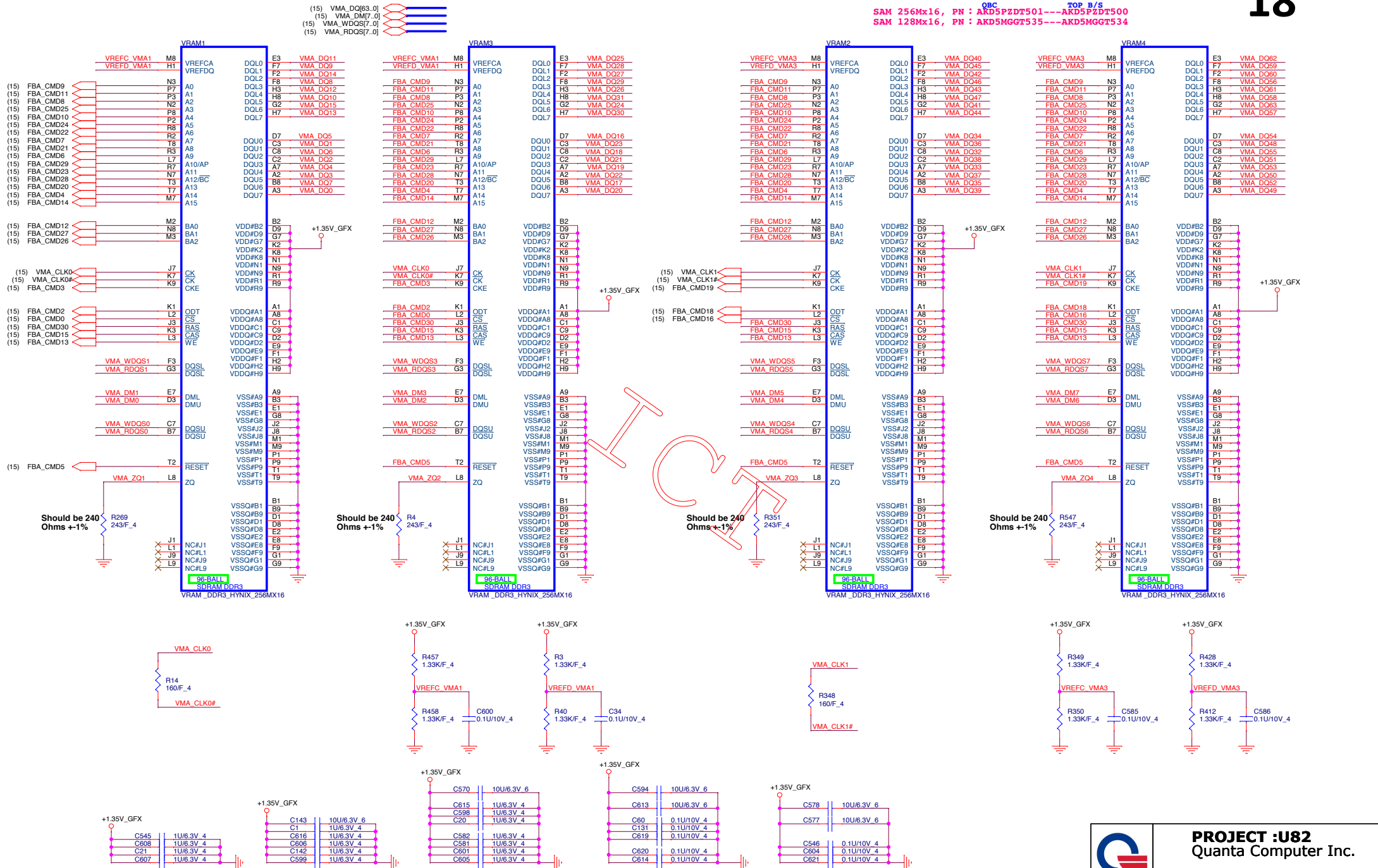


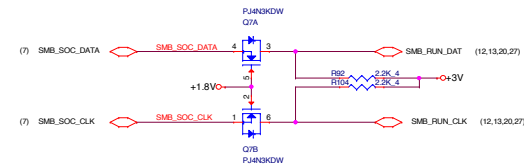
# CHANNEL A: 256MB/512MB DDR3

HYU 256Mx16, PN : AKD5PGWT08---AKD5PGWT07  
HYU 128Mx16, PN : AKD5MZDTW03---AKD5MZDTW02


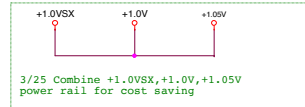
SAM 256Mx16, PN : AKD5PZDT501---AKD5PZDT500  
SAM 128Mx16, PN : AKD5MGGT535---AKD5MGGT534

18

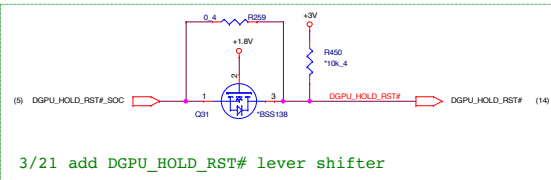




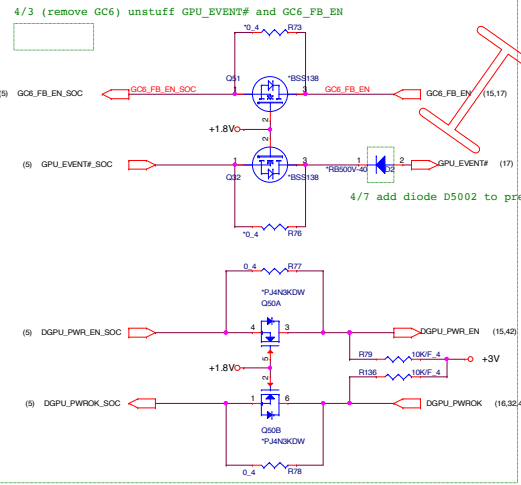
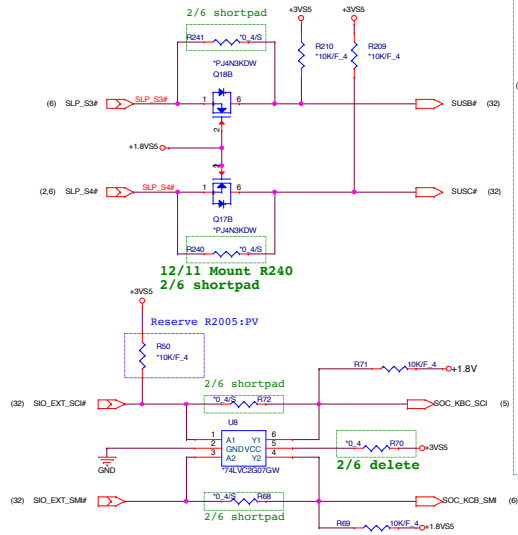
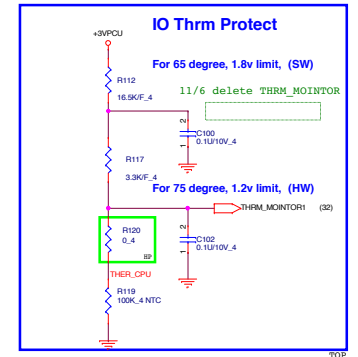
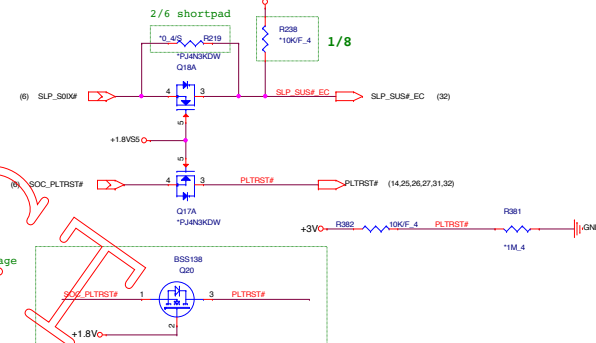
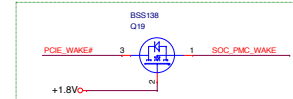
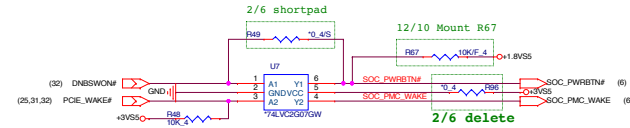
#### 11/4 Delete deplicate TP lever shift



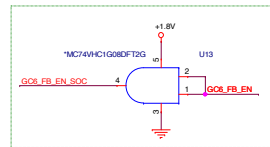
3/25 Combine +1.35VSFR,+1.35V power rail for cost saving



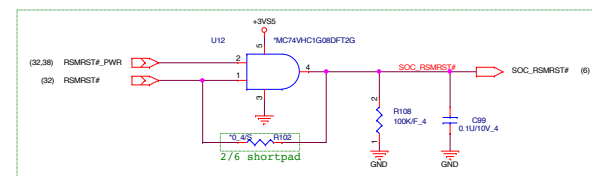
```
3/21 add DGPU_HOLD_RST# lever shifter
```



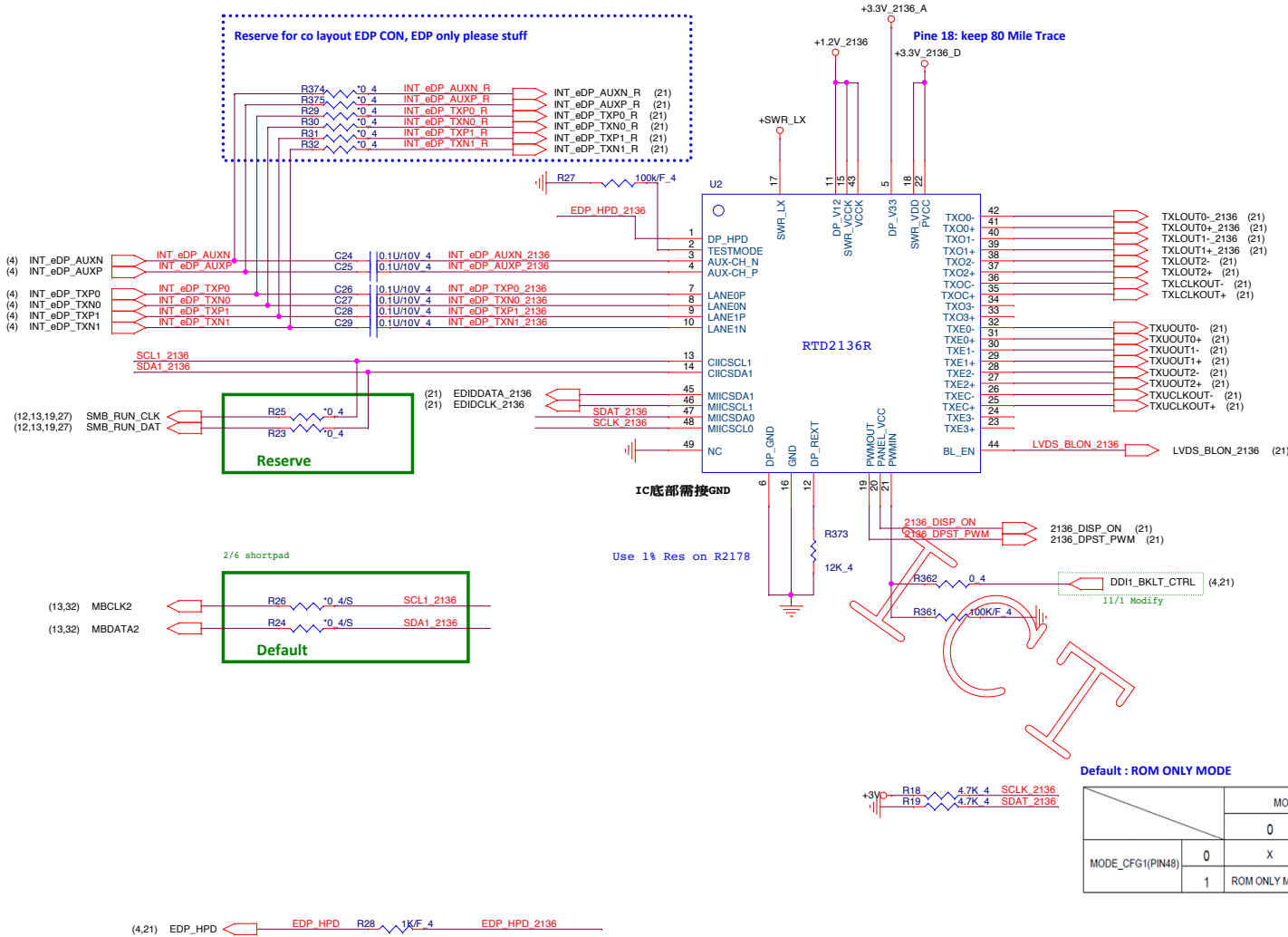
3/28 add level shifter for GPU GPIO



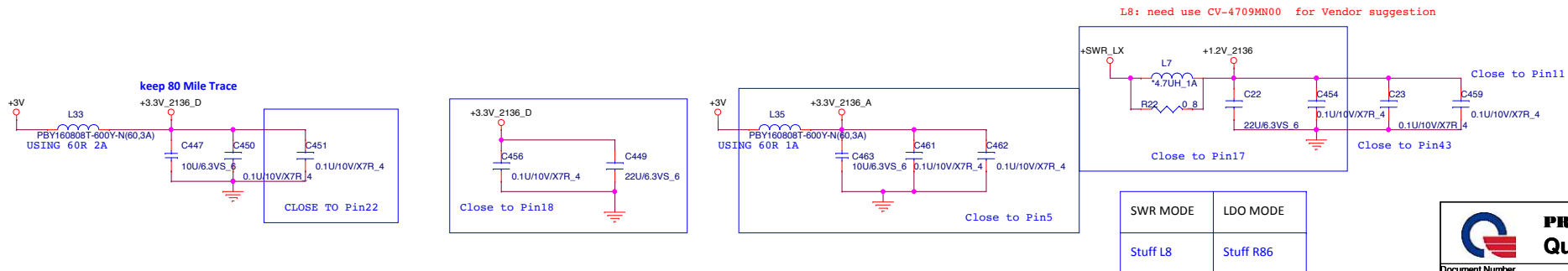
4/2 reserved an And gate to avoid voltage divider circuit from nvidia suggestion (the AND gate need to be replaced to +1.8V Vcc driven)

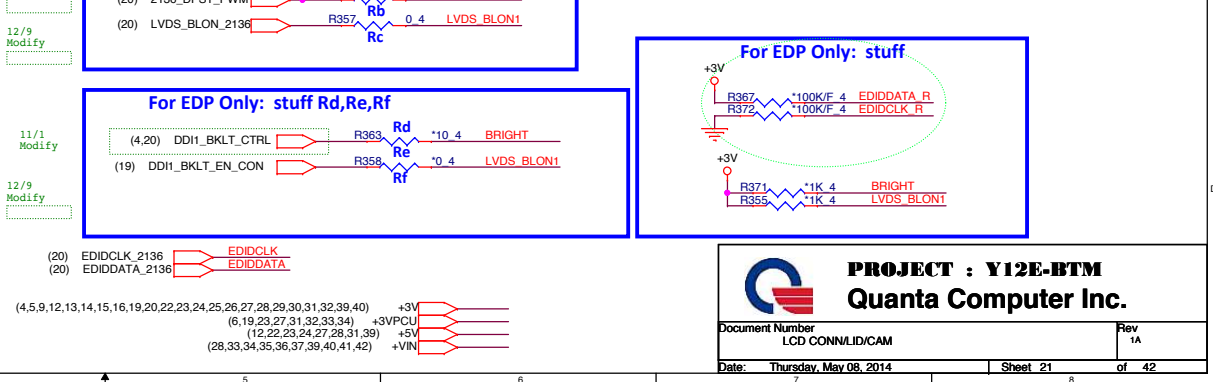
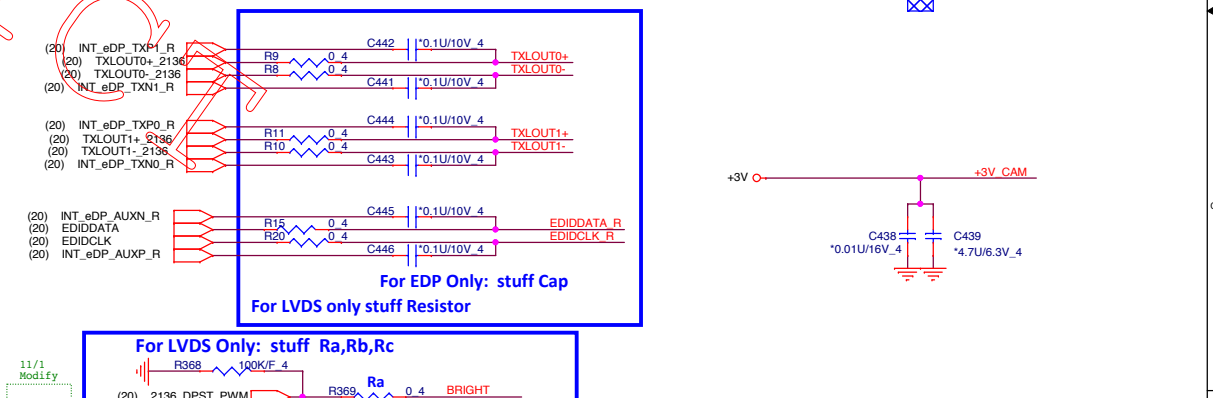
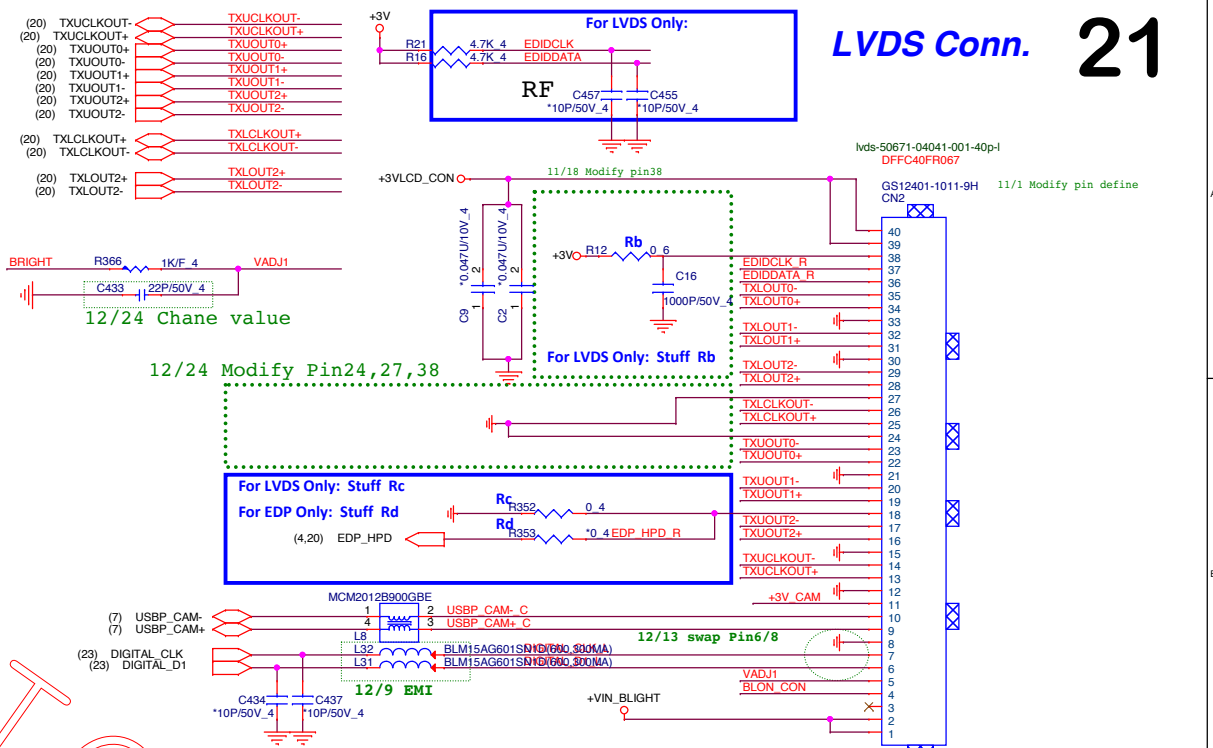
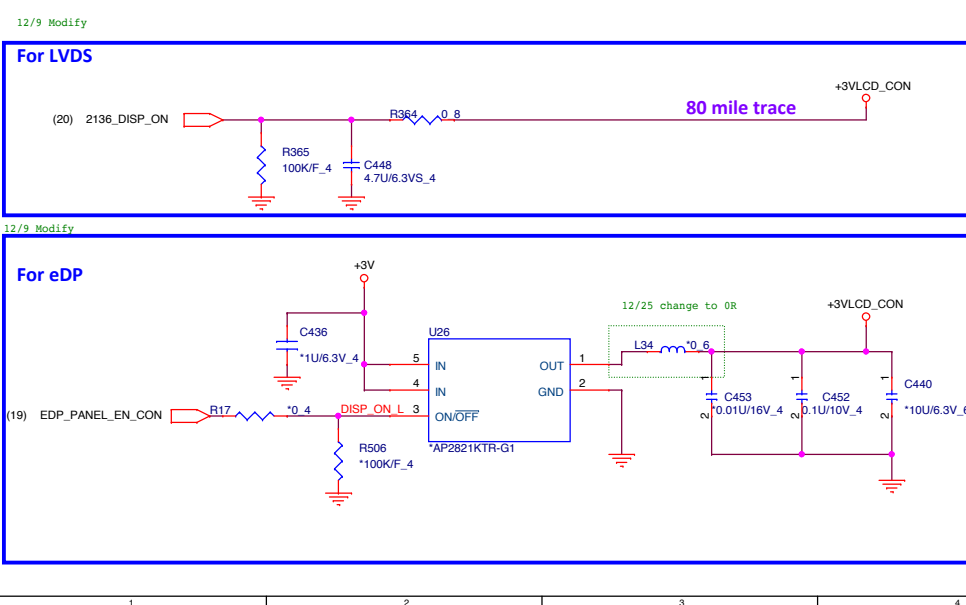
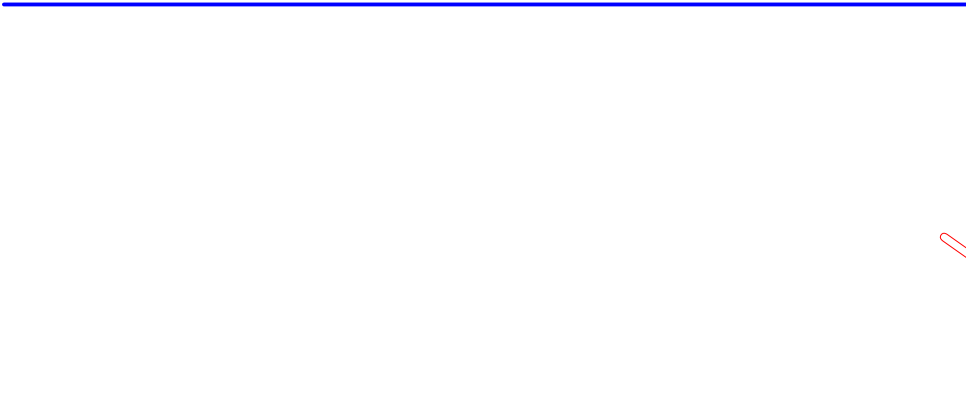
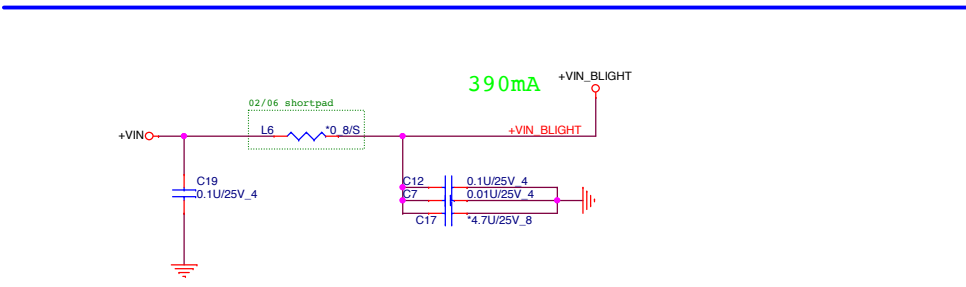
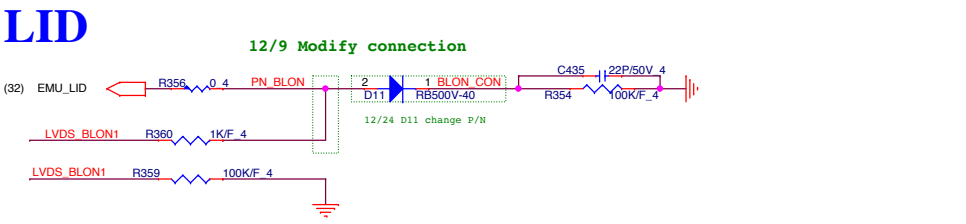


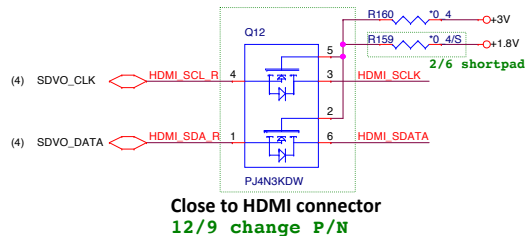
11/5 Add AND gate



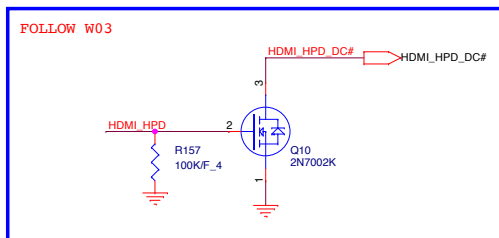
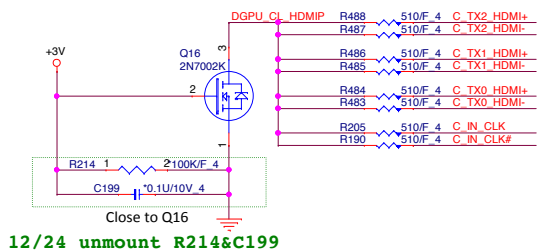
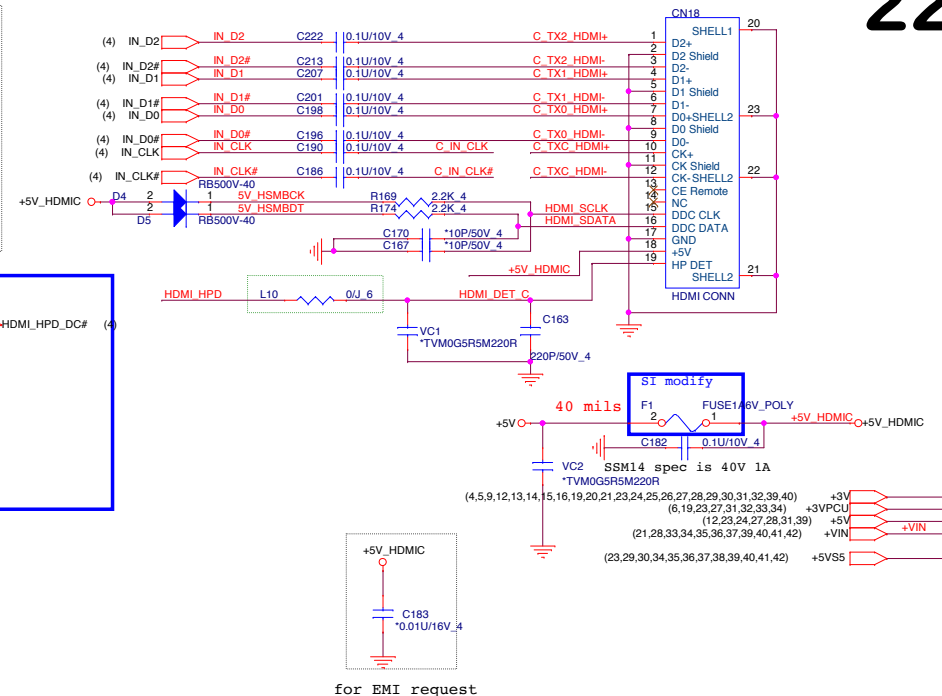
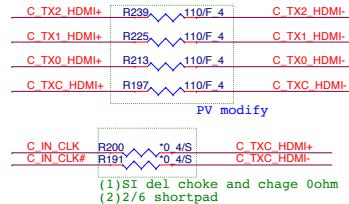
		MODE_CFG0(PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE



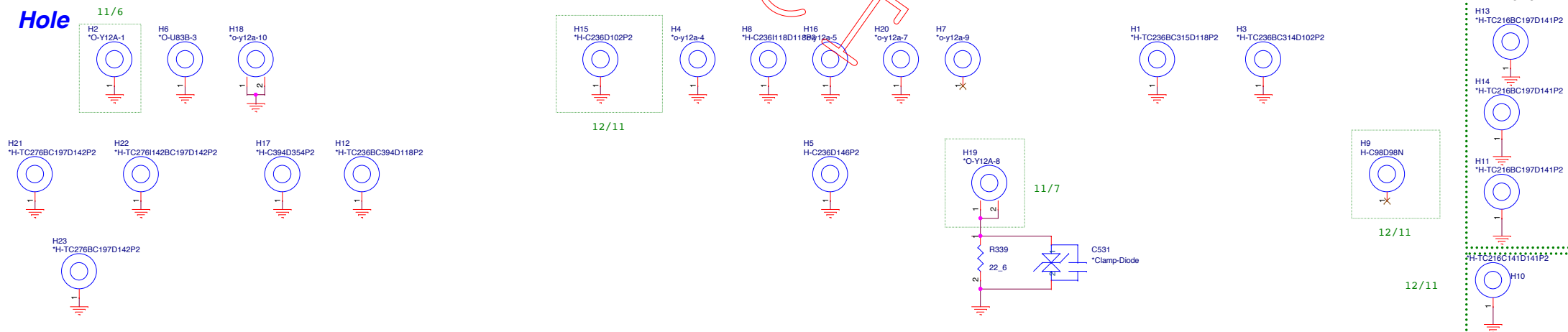
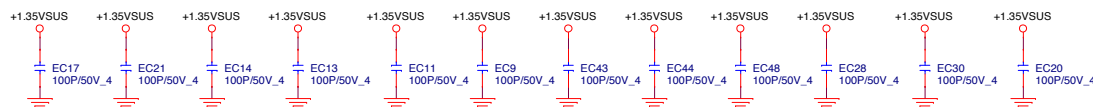




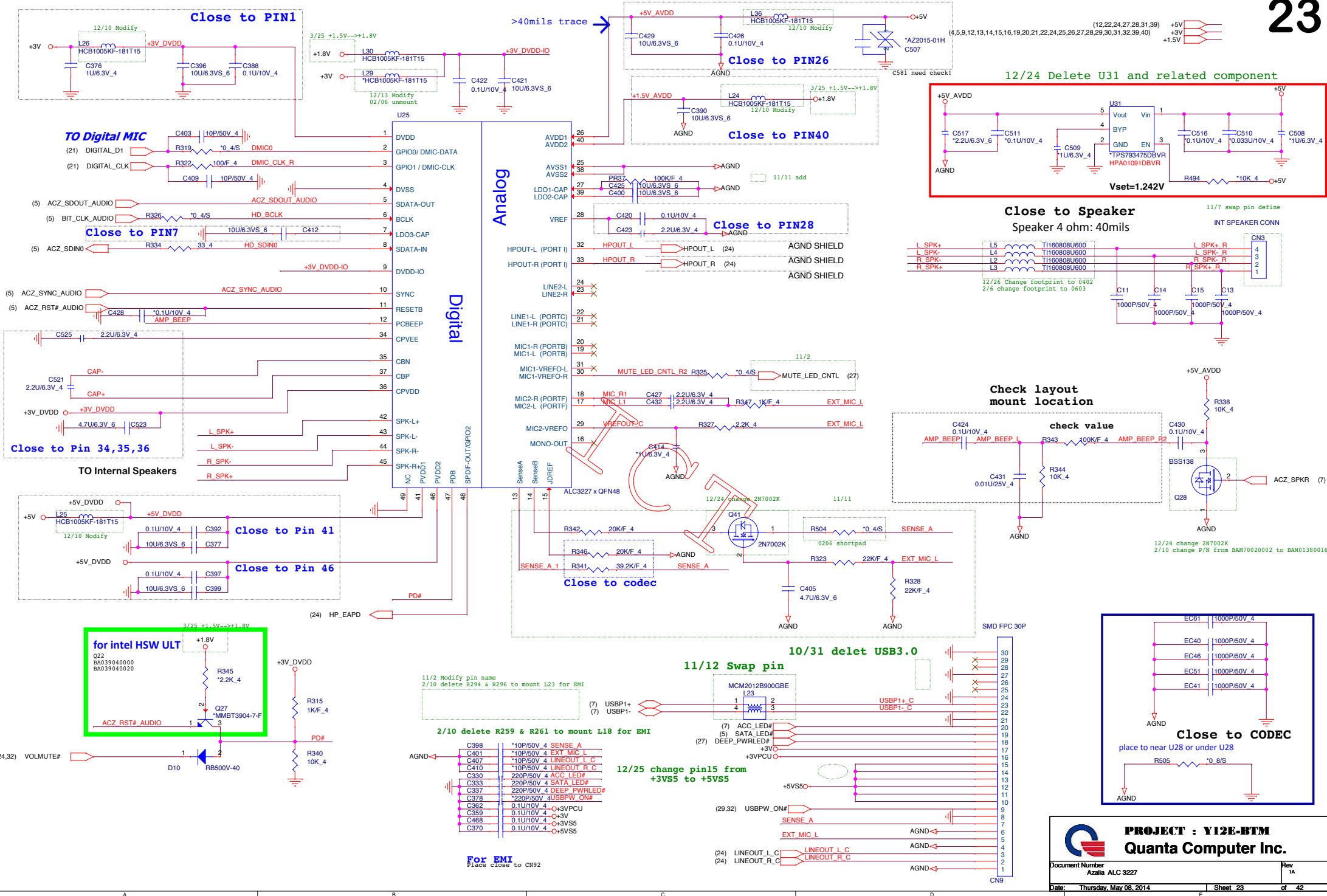
## EMI Solution

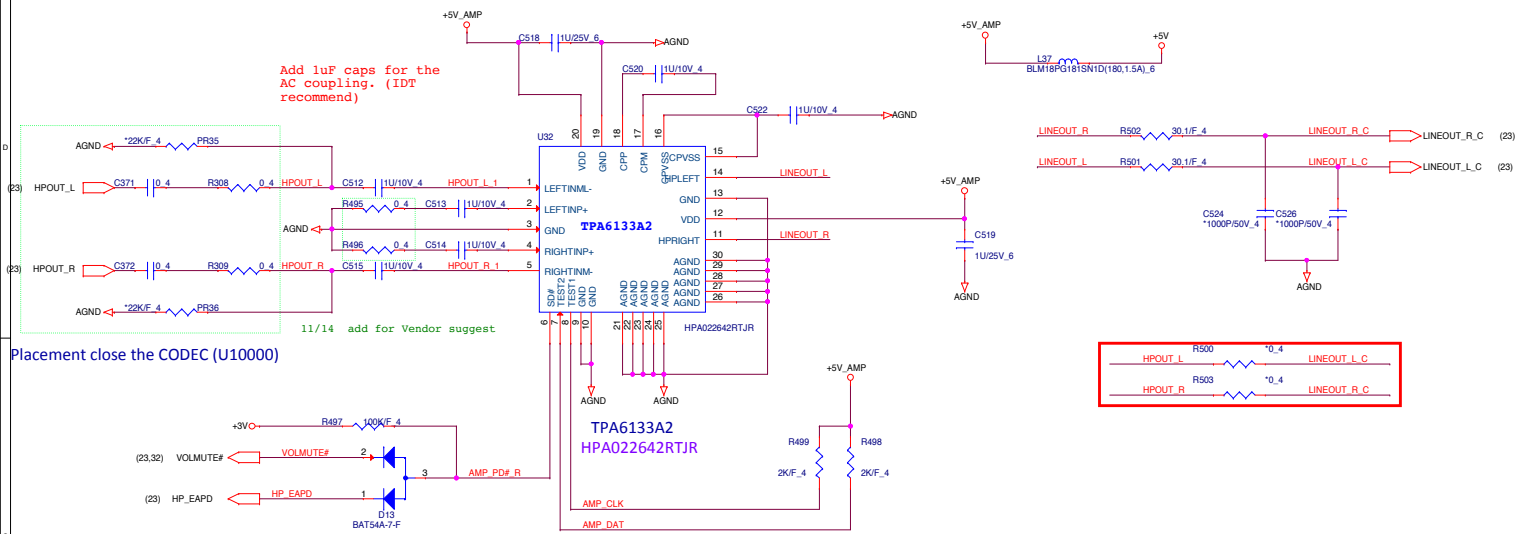


**Hole**

**EMI**





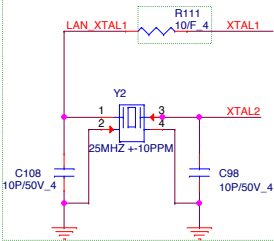


IDT

For EMI 0 - 22 ohm

10/31 add crystal

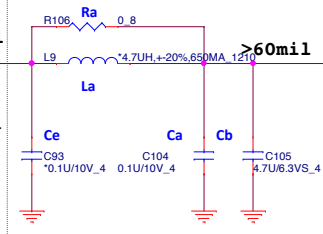
Change Y1 PN to BG625000121: PV



Power trace Layout 宽度 &gt; 60mil

&gt;60mil

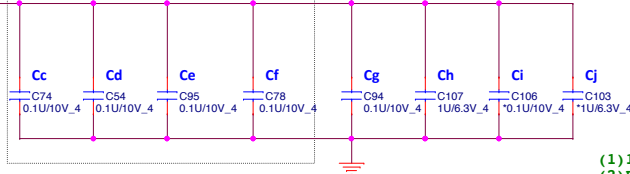
&gt;60mil

Trace < 30 mil  
Width > 60 milFor GbE  
Stuff La, Ca, CbFor 10/100  
NA: La, Ca, Cb  
STUFF: Ra, Ce

For GbE

\* Place Cc, Cd, Ce, Cf  
close to each VDD10 pin-- 3, 22, 8, 30

For 10/100 NA Ce, Cf

\* Place Ce, Cf  
close to each VDD10 pin-- 8, 30 only,

For GbE

\* Place Cg and Gh close to each VDD10 pin-- 22

For 10/100

\* Place Ci and Cj close to each VDD10 pin-- 30

11/10 Modify name

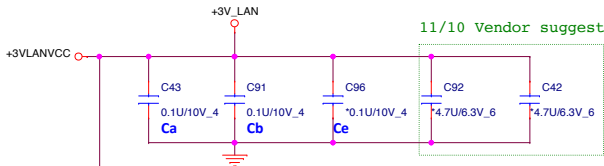
For GbE Stuff U3, U4  
For 10/100 Stuff U3

For 10/100

\* Stuff Cb and Ce only, close to each VDD33 pin-- 23, 32

For GIGA

\* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



11/10 Vendor suggest

\* Place Cc and Cd close to each VDD33 pin-- 23

For GIGA  
Stuff Cc, Cd

For 10/100

NA: Cc, Cd

Remove For Not Using SWR mode

For GiGA

BOT: GST5009B LF, DB0206LAN00

FCE: NS892407, DB0LL1LAN00

For 10/100

BOT: TST1284R LF DB0EL5LAN00

FCE: NS892408, DB0EF7LAN01

(4,5,9,12,13,14,15,16,19,20,21,22,23,24,26,27,28,29,30,31,32,39,40)

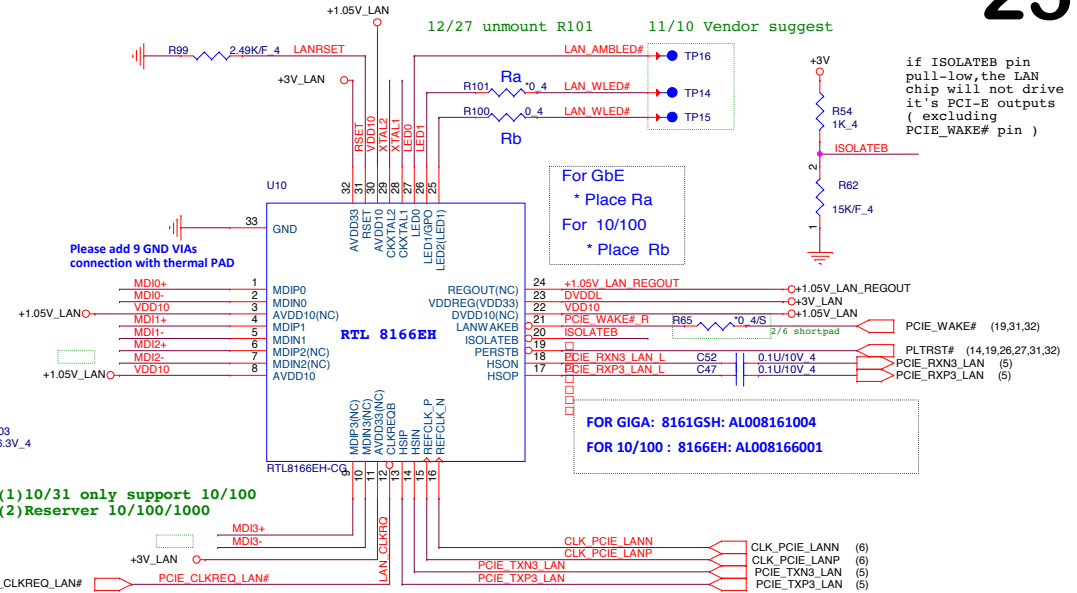
+3V  
+3V\_LANVCC

(39)

+1.05V\_LAN

12/27 unmount R101

11/10 Vendor suggest

if ISOLATED pin  
pull-low, the LAN  
chip will not drive  
it's PCI-E outputs  
( excluding  
PCI-E\_WAKE# pin )

For GbE

\* Place Ra

For 10/100

\* Place Rb

FOR GIGA: 8161GSH: AL008161004  
FOR 10/100: 8166EH: AL008166001(1) 10/31 only support 10/100  
(2) Reserver 10/100/1000

(5) PCIE\_CLKREQ\_LAN#

+3V\_LANVCC

+3V\_LANVCC

12/24 change to 1%

RJ45

(White)

LAN\_WLED#

LAN\_WLED#

LED\_White\_P

LED\_White\_N

RX1+

RX0-

TX1+

TX0+

TX0-

TX0+

LED\_AMB\_P #1

LED\_AMB\_N #2

RJ45\_CONN

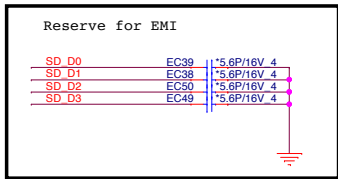
(Amber)

(1) 10/31 Delete 10/100  
 (2) Change RJ45 P/N for U83B  
 (3) 11/7 Reserver 10/100/1000  
 (4) 12/17 EMI reserve TX2+/- & TX3+/- R and C.  
 (5) Change LAN CONN P/N & footprint

PROJECT : Y12E-ITM  
Quanta Computer Inc.Document Number  
RTL 8161/RJ45Rev  
1A

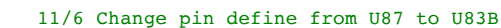
Date: Thursday, May 08, 2014

Sheet 25 of 42



## Share Pin

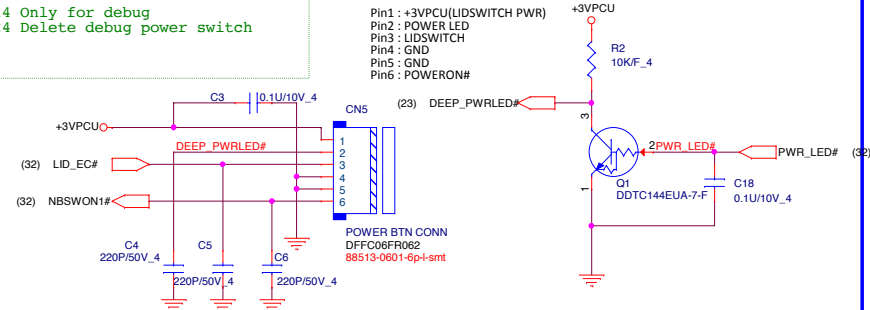
SD / MMC



Change footprint to  
sdcard-psdbtc-09glbs1nn4h3-11p

## Power Button Connector

11/14 Only for debug  
12/24 Delete debug power switch

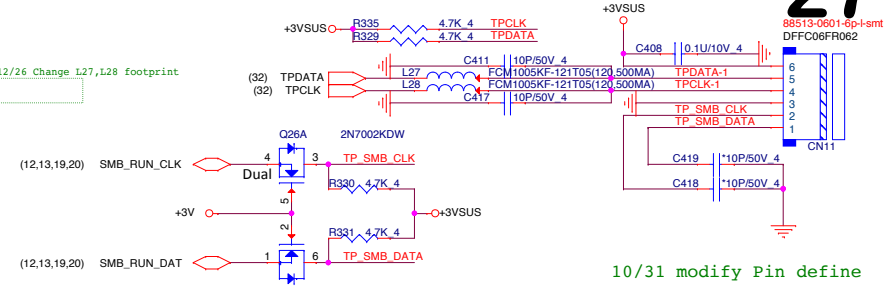


## Lid Switch FOR 15"

11/2 delete LID switch

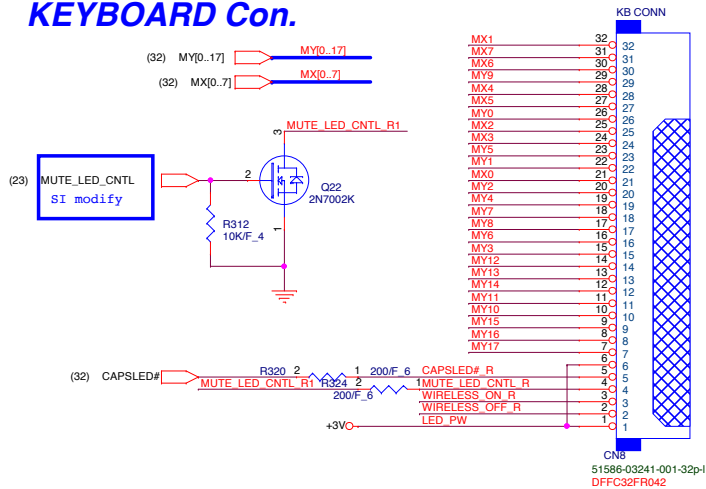
## Touch Pad Connector

12/26 Change L27,L28 footprint

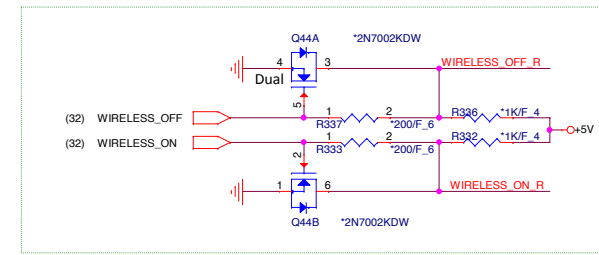
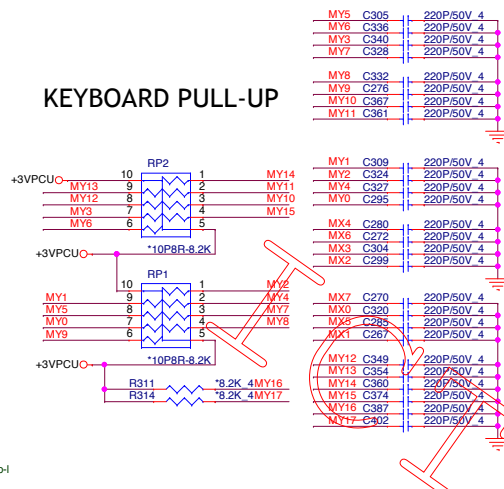


10/31 modify Pin define

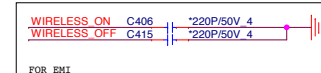
## KEYBOARD Con.



## KEYBOARD PULL-UP



12/24 Combine to Dual MOS



11/7 Delete backlight KB

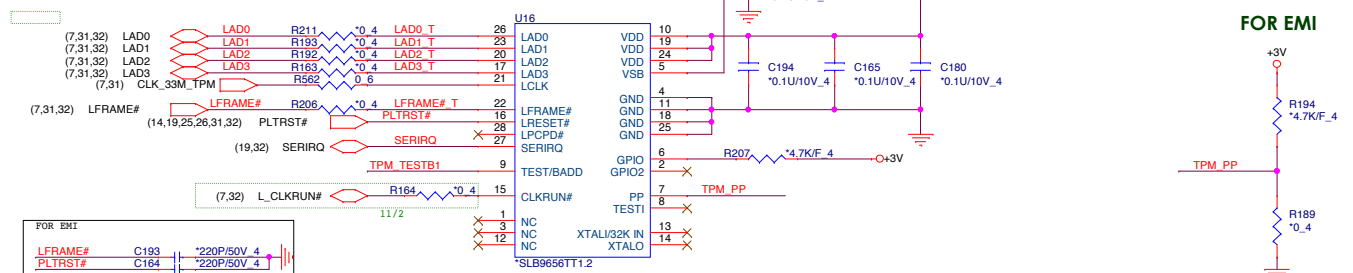
## 2/6 Unmount TPM and its related component

### TPM (1.2)

Address

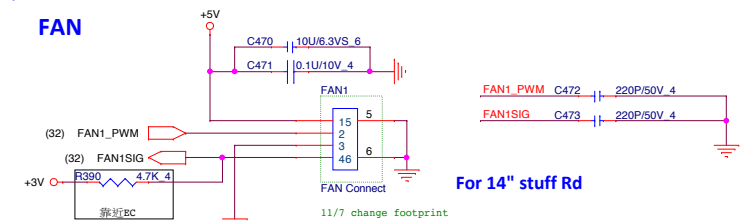
	BADD
HIGH	4EH/4F (default)

5/6 R562 for LPC\_CLK 3 branches, should be 12.5ohm



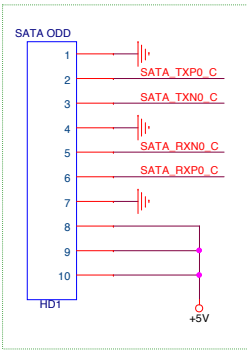
FOR EMI

## FAN



# SATA HDD Connector(Cable type) 14", 15", 17"

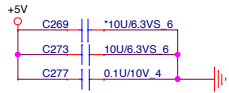
+5V: 2 A(4 Pin)  
Gnd : (5 Pin)  
+3V: 2 A(4 Pin)



SATA_TXP0_C C302	0.01U/16V_4	SATA_TXP0 (5)
SATA_TXN0_C C298	0.01U/16V_4	SATA_TXN0 (5)
SATA_RXN0_C C294	0.01U/16V_4	SATA_RXN0 (5)
SATA_RXP0_C C282	0.01U/16V_4	SATA_RXP0 (5)

11/12 delete 14" and 15" SATA CONN

11/1 Modify pin define and footprint  
11/11 Swap pin  
12/25 change footprint

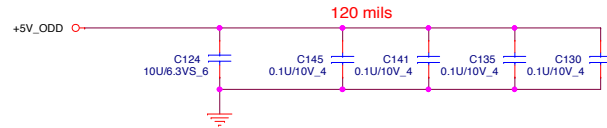
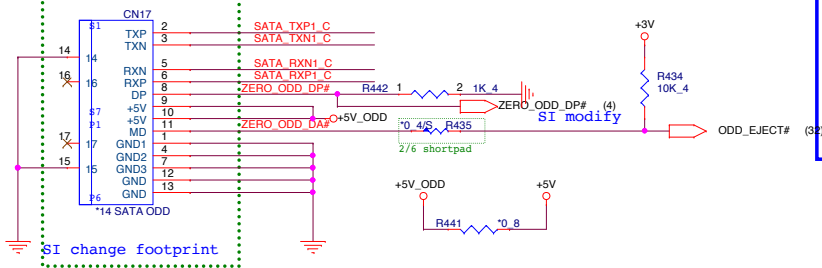


## SATA ODD CONNECTOR

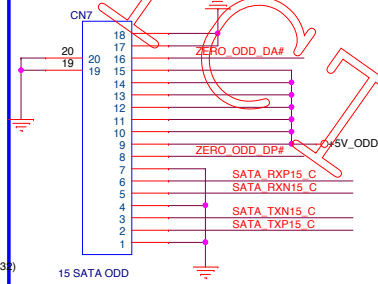
### 14" SATA ODD

12/24 update footprint

Bypass CAP close conn



### 15" & 17" SATA ODD New Type



11/6 update footprint

11/1 Colayout 15" & 17" ODD

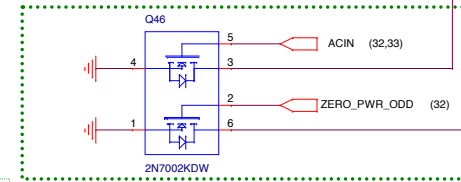
For 15" & 17": stuff Ra

11/11 Swap pin

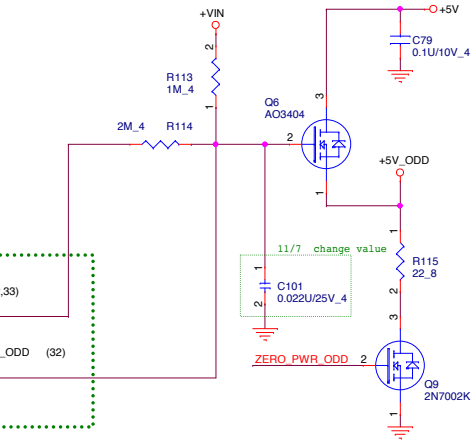
SATA_TXP15_C C494	0.01U/25V_4	SATA_TXP1 (5)
SATA_TXN15_C C491	0.01U/25V_4	SATA_TXN1 (5)
SATA_RXN15_C C489	0.01U/25V_4	SATA_RXN1 (5)
SATA_RXP15_C C487	0.01U/25V_4	SATA_RXP1 (5)

For 14": stuff Rb

SATA_TXP1_C C495	0.01U/25V_4	SATA_TXP1
SATA_TXN1_C C492	0.01U/25V_4	SATA_TXN1
SATA_RXN1_C C490	0.01U/25V_4	SATA_RXN1
SATA_RXP1_C C488	0.01U/25V_4	SATA_RXP1



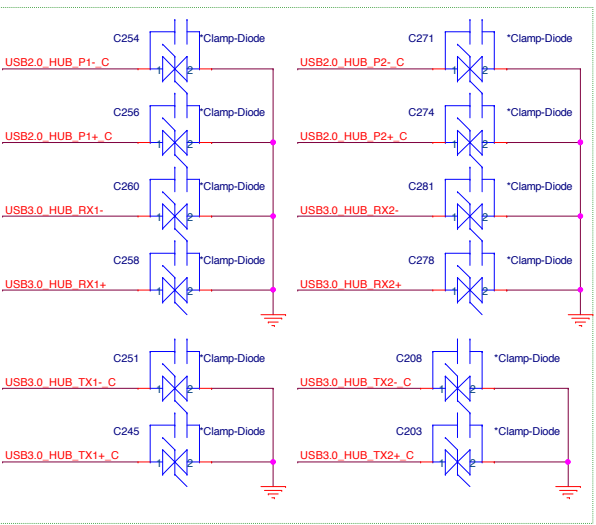
12/24 change to dual MOS



For BM1

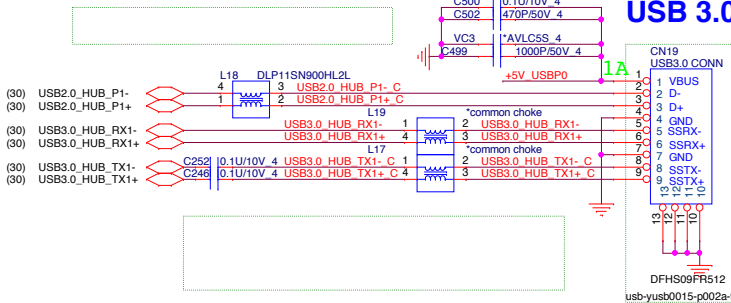
ACIN C223	*220P/50V_4
ZERO_PWR_ODD C214	*220P/50V_4

USB 2.0/3.0 Combo



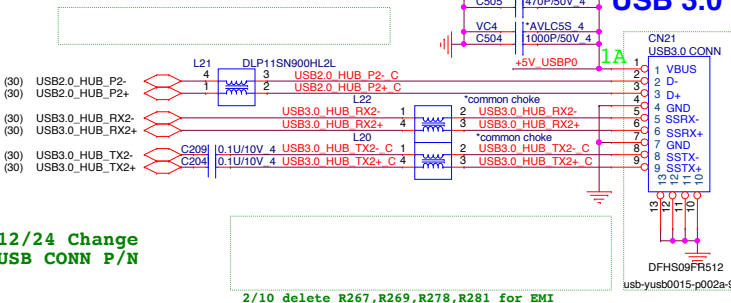
11/1 modify

2/10 delete R259 & R261 to mount L18 for EMI



USB 3.0

2/10 delete R271 & R275 to mount L21 for EMI



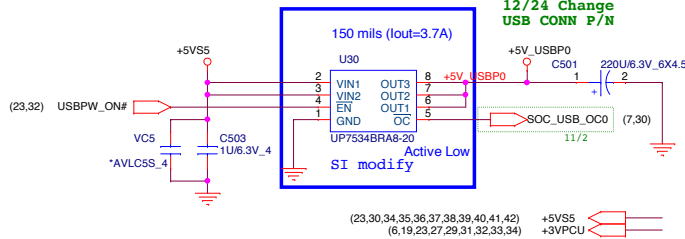
USB 3.0

29

12/24 Change USB CONN P/N

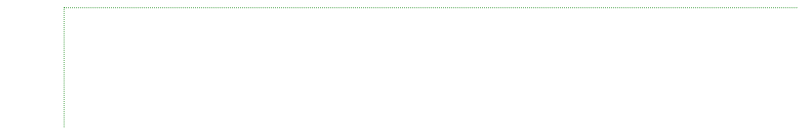
11/12 modify

10/31 delet USB3.0 Charger IC



12/24 Change USB CONN P/N

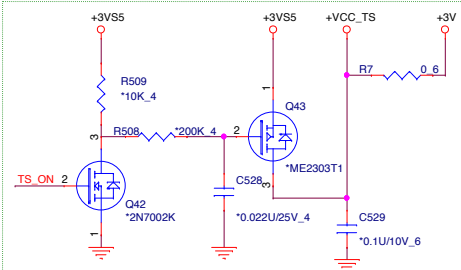
Leap Motion 11/7 Delete Leap motion



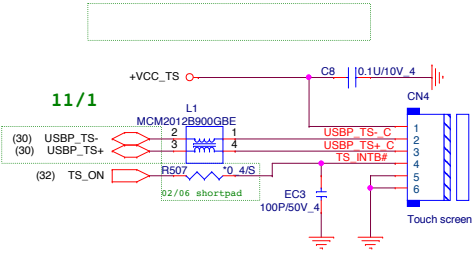
Fingerprint Conn 11/7 Delete Fingerprint CONN



Touch screen 12/24 modify control schematic

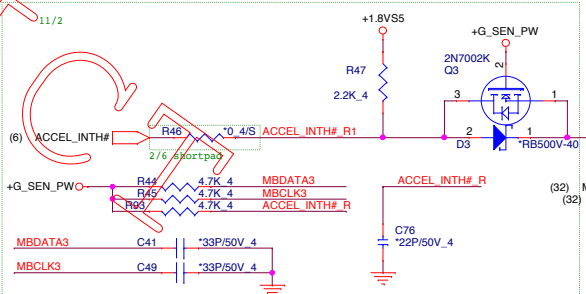


2/10 delete R3 & R4 to mount L1 for EMI

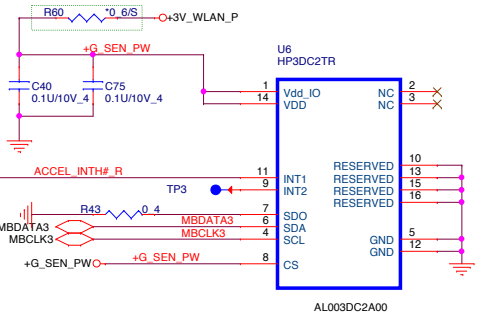


11/1

Accelerometer Sensor 沿用U82



2/6 shortpad



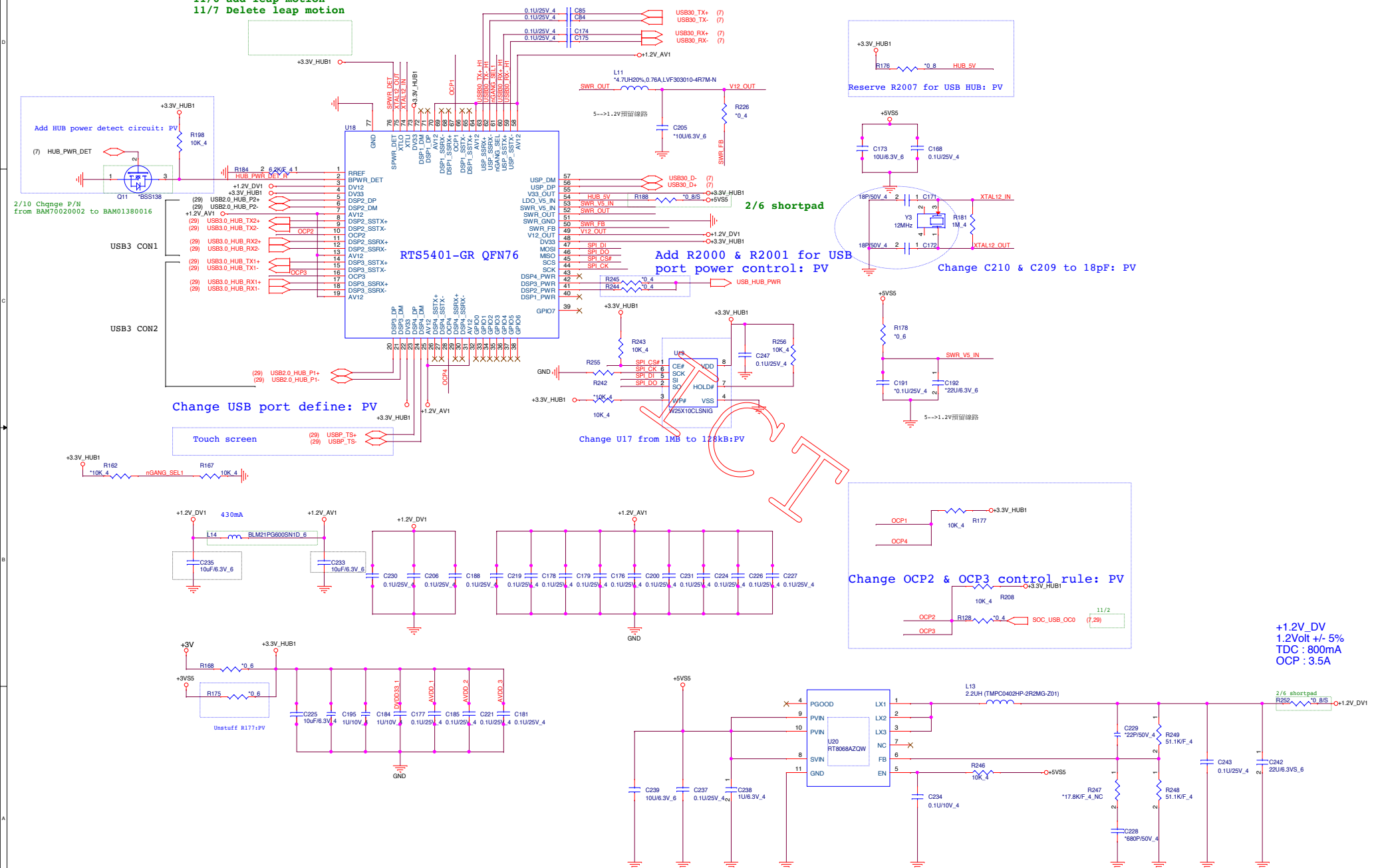
Green CLK Circuitry

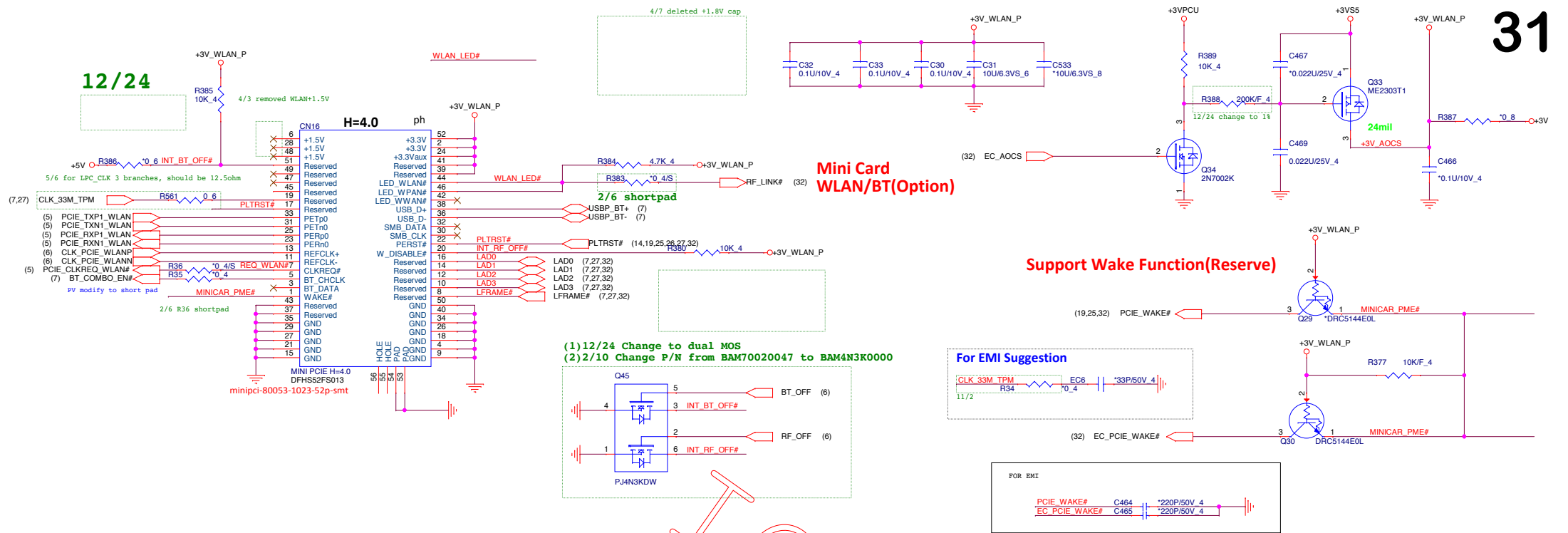
10/30 delete Green Clock

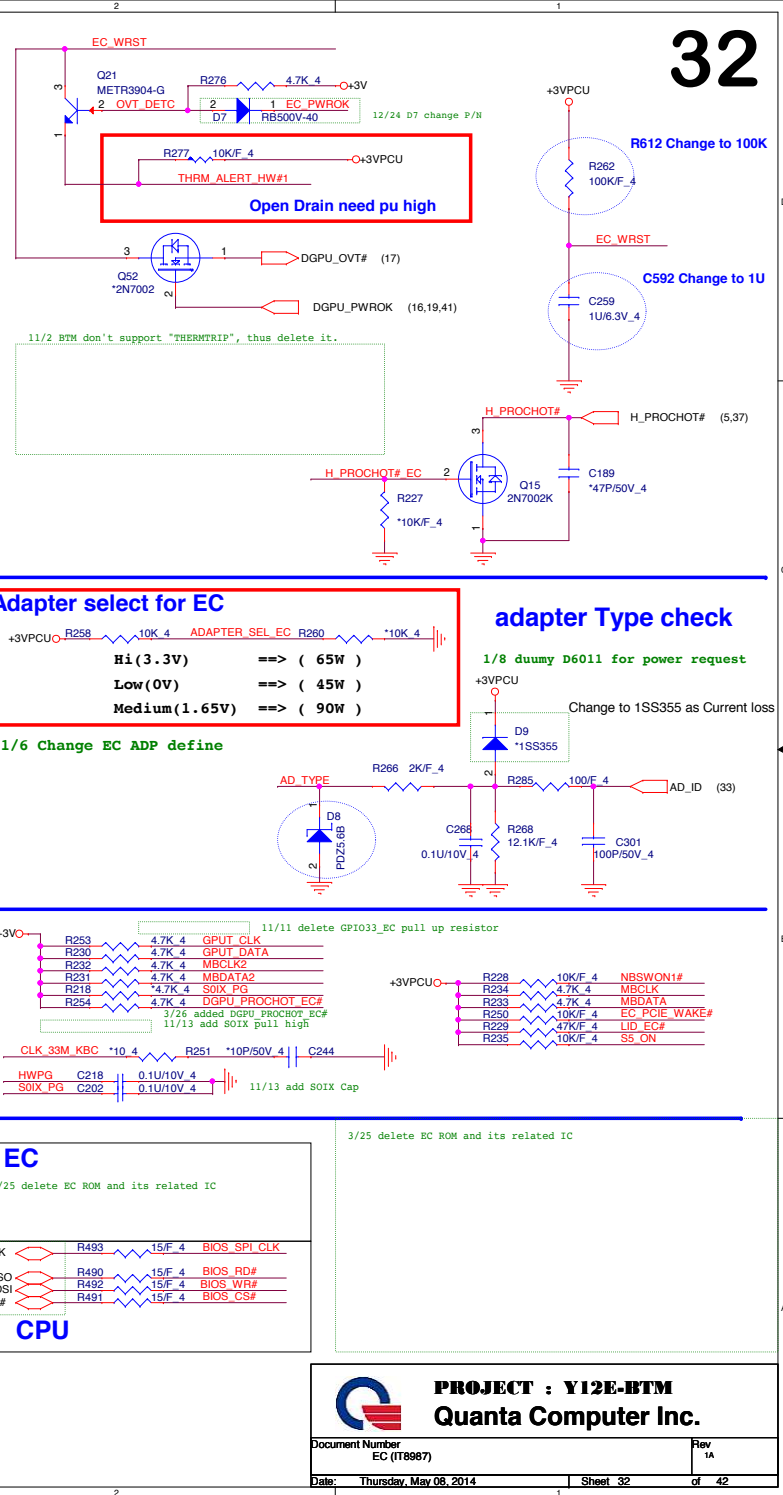




```
11/6 add leap motion
11/7 Delete leap motion
```

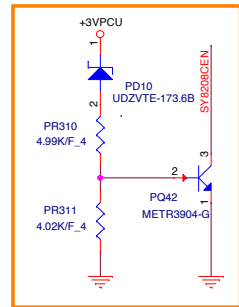






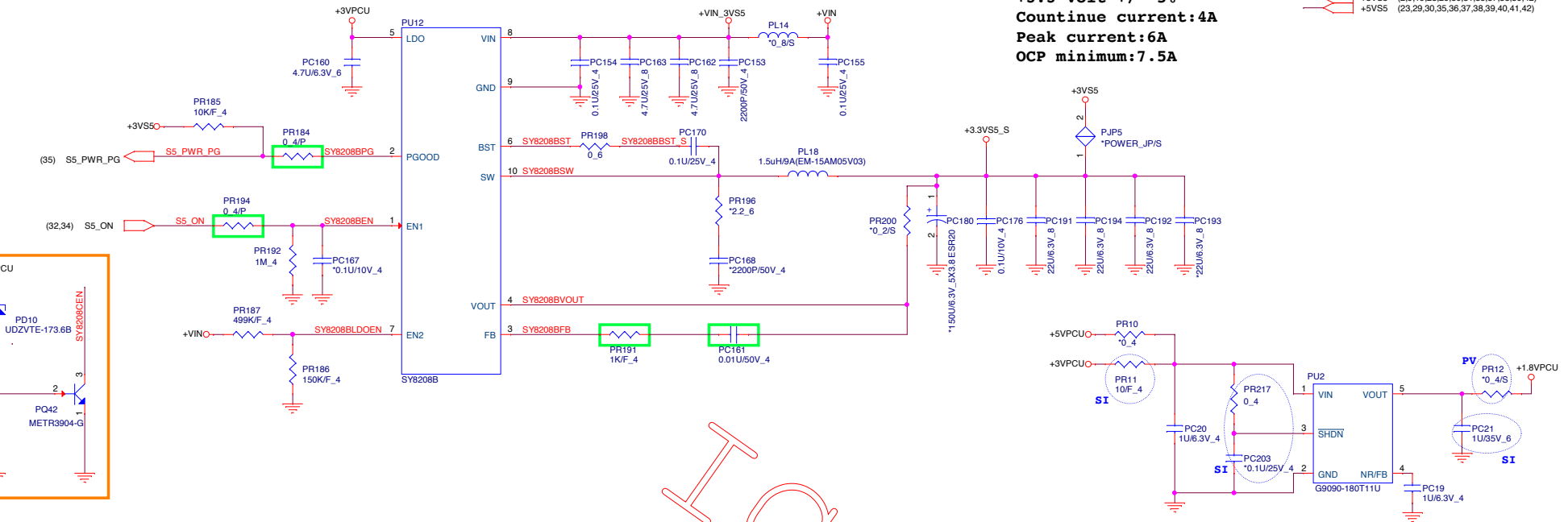


## DC/DC +3VS5/+5VS5

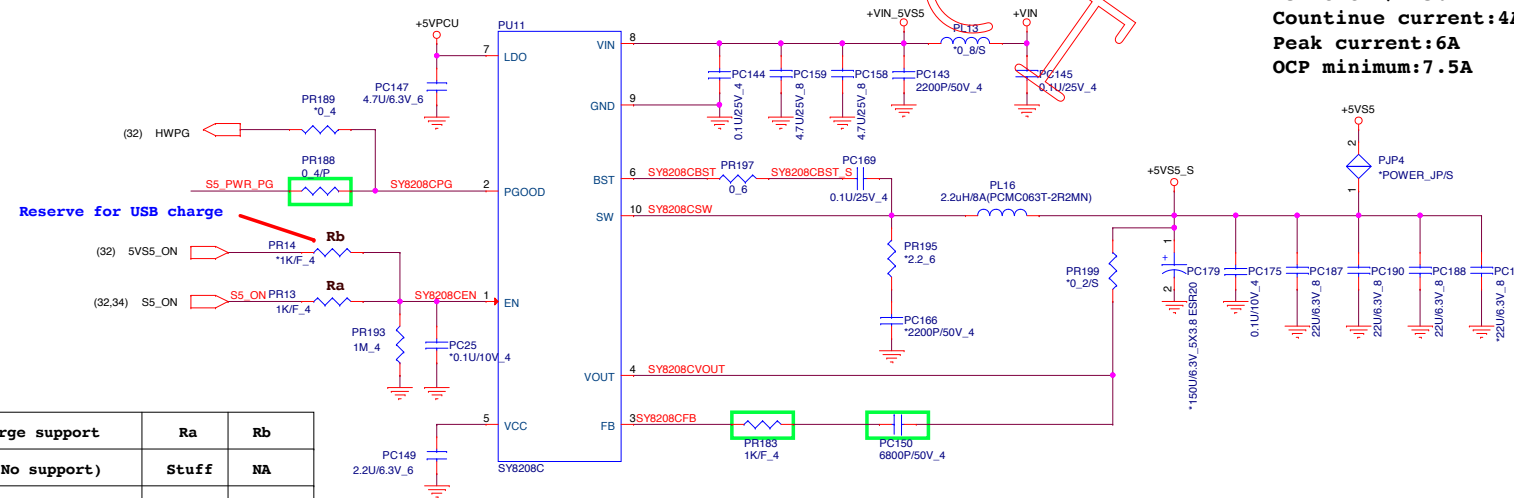


**+3.3 Volt +/- 5%**  
**Countinue current:4A**  
**Peak current:6A**  
**OCP minimum:7.5A**

+3VS5 (2,9,19,23,29,30,31,35,37,38,39,42)  
 +5VS5 (23,29,30,35,36,37,38,39,40,41,42)

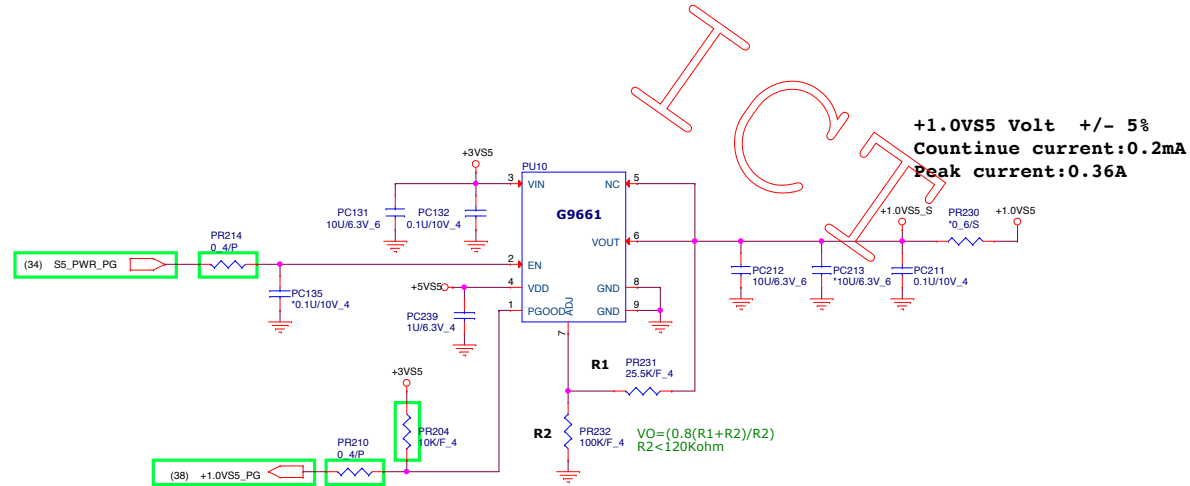
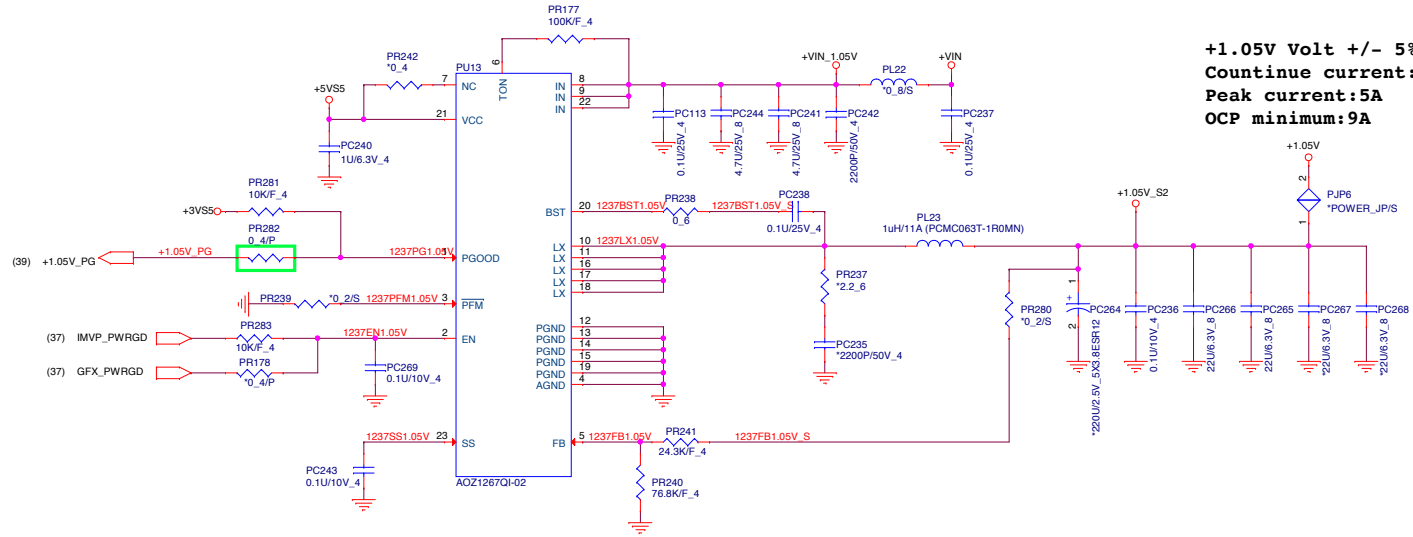


**+5 Volt +/- 5%**  
**Countinue current:4A**  
**Peak current:6A**  
**OCP minimum:7.5A**



Reserve for USB charge

USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff



**PROJECT : Y12E-BTM**  
**Quanta Computer Inc.**

Document Number  
 +1.05V/+1.5V (SY8002)

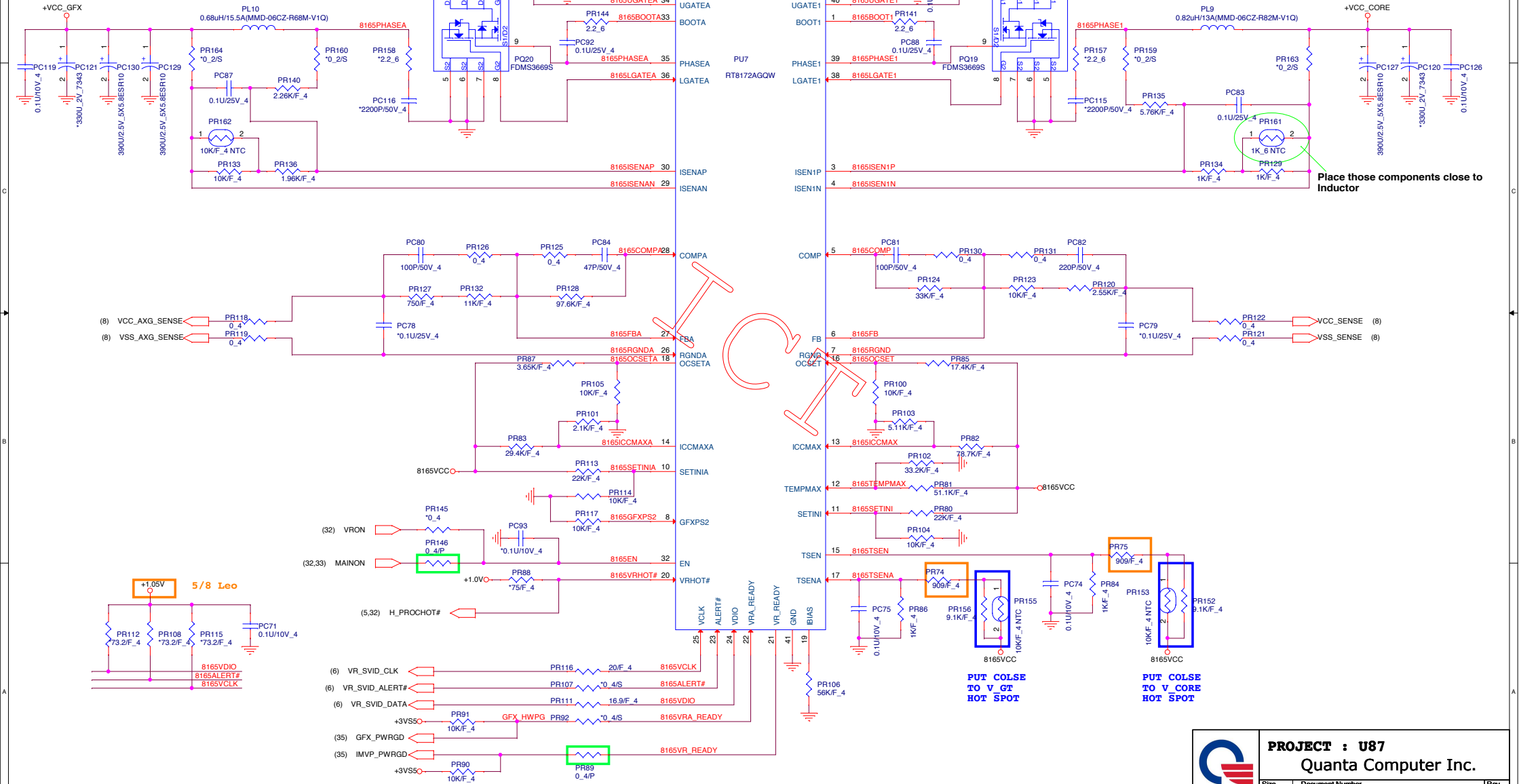
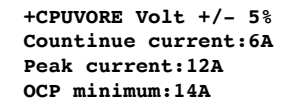
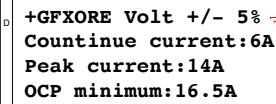
Rev  
 1A

Date: Thursday, May 08, 2014

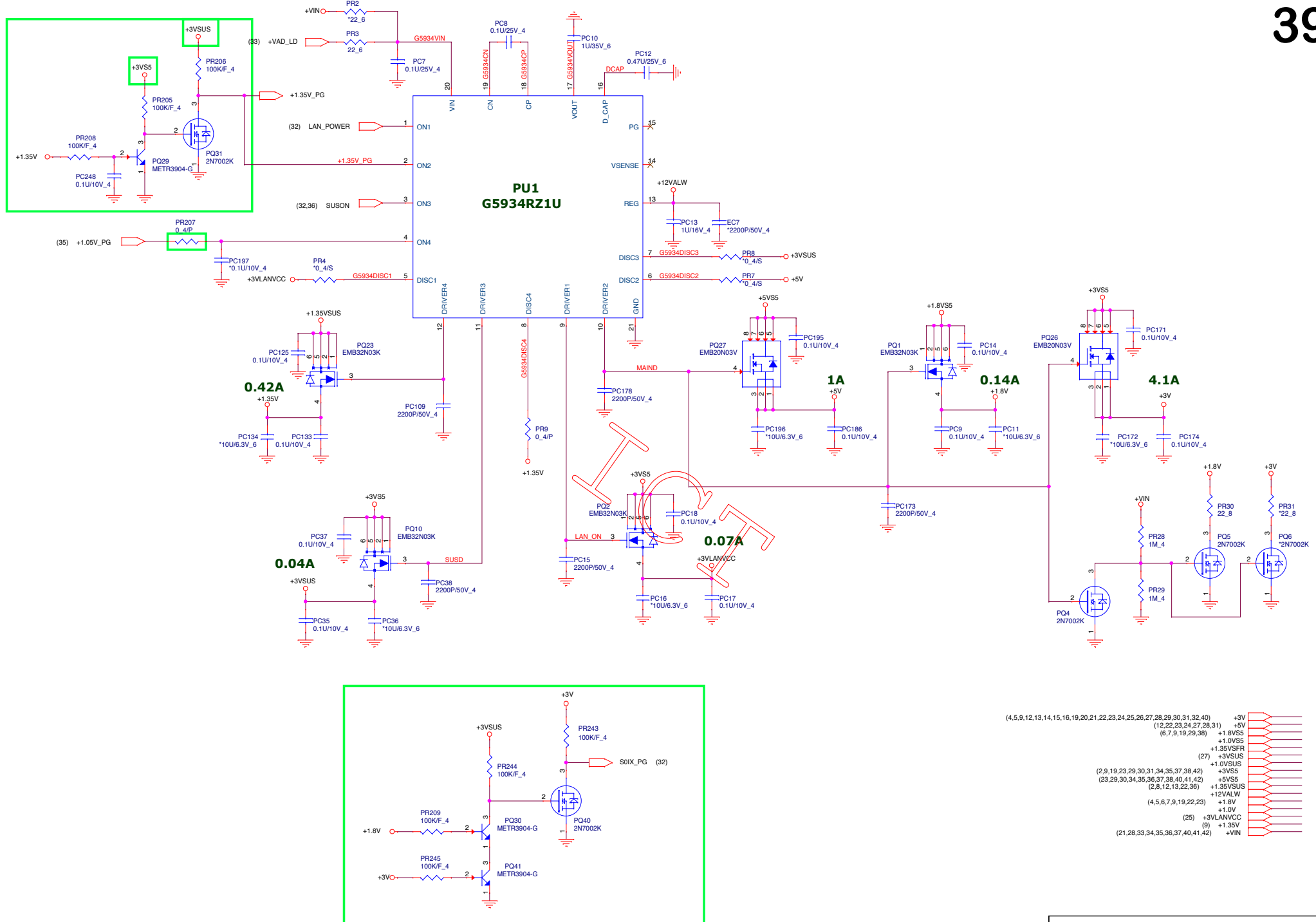
Sheet 35 of 42



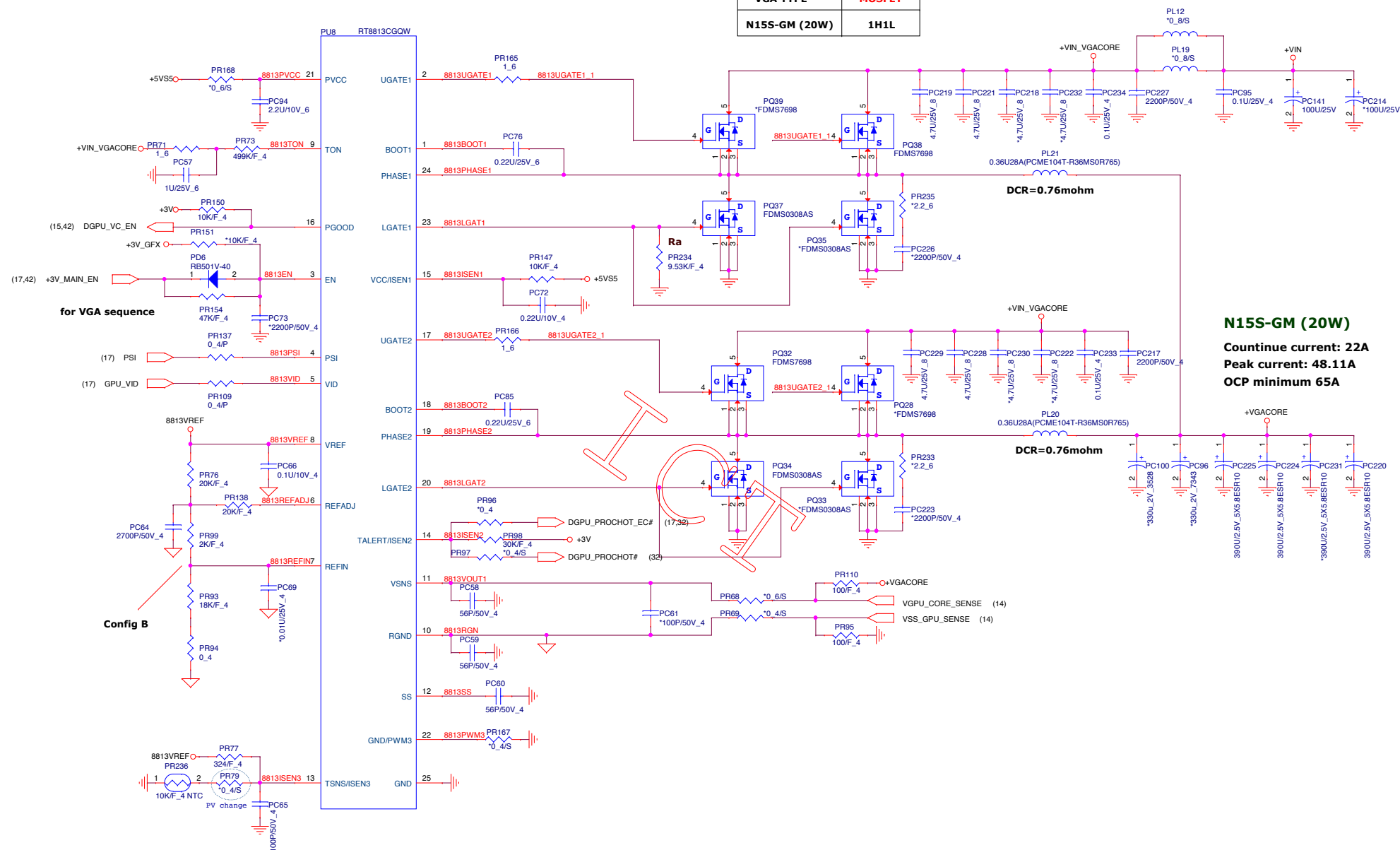








<b>VGA TYPE</b>	<b>MOSFET</b>
<b>N15S-GM (20W)</b>	<b>1H1L</b>



**N15S-GM (20W)**  
 Countinue current: 22A  
 Peak current: 48.11A  
 OCP minimum 65A

